Design of Robust CAN-FD Networks

An automated Model based Design Flow

Federico Pereira

Agenda

- Design flow introduction
- Topology simulation
- Validation criteria
- Need for automatization
- Conclusion

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Design flow introduction (1/2)

Why should I simulate?

- Constant increase of quality and performance in todays requirements within in-vehicle networks (IVN) systems
- Quality assurance
- Further analysis compared to laboratory test
- Total cost reduction

We consider simulation as the most important phase in validating a modern topology

Design flow introduction (2/2)

3 main steps are distinguished in this kind of design flow:

- **Topology simulation**
  - Virtual network prototype
- **Laboratory measurements**
  - Real network test
- **Verification**
  - Comparison between the virtual measurements and real measurements

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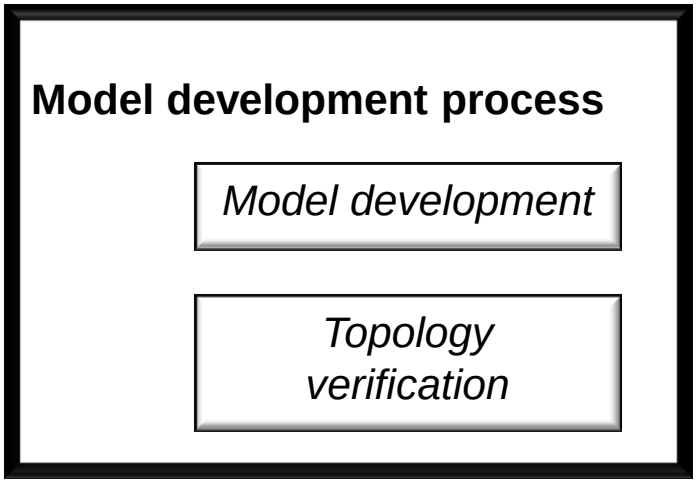
Topology validation – Model development

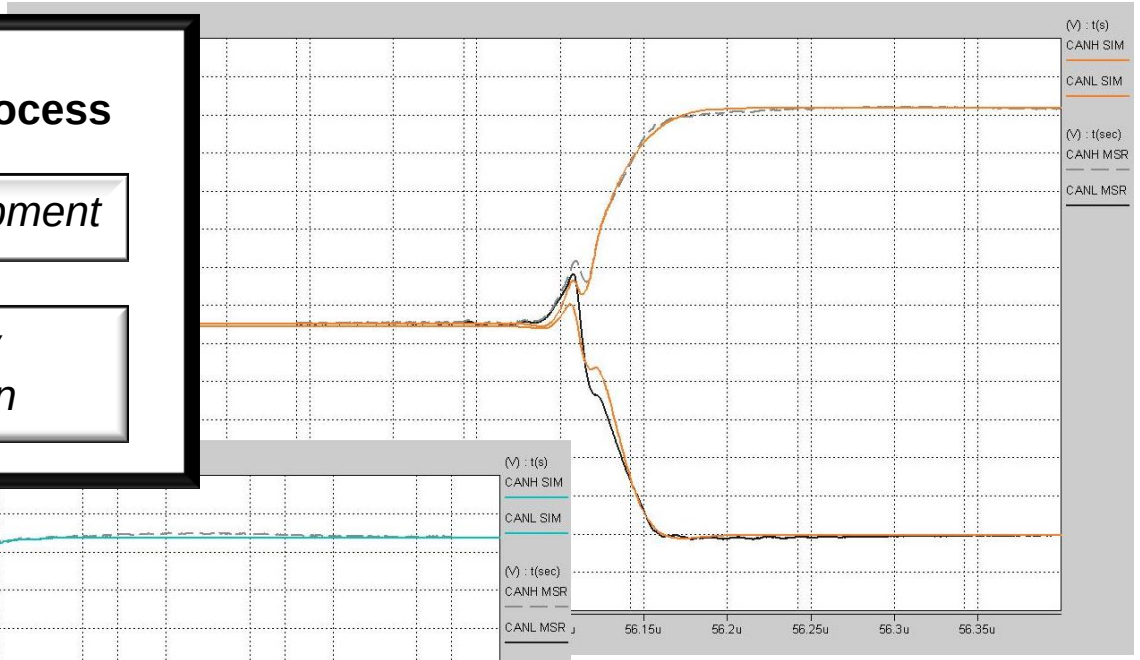


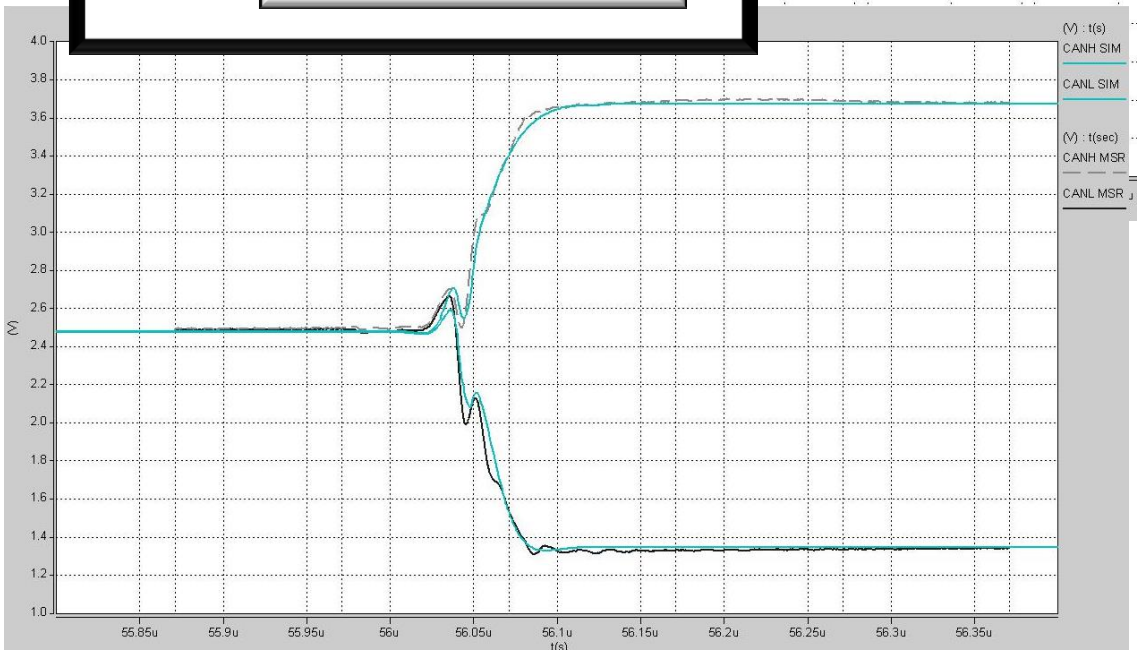
Topology validation – Model development

Model development process

Model development

Topology verification





Topology validation – Model development

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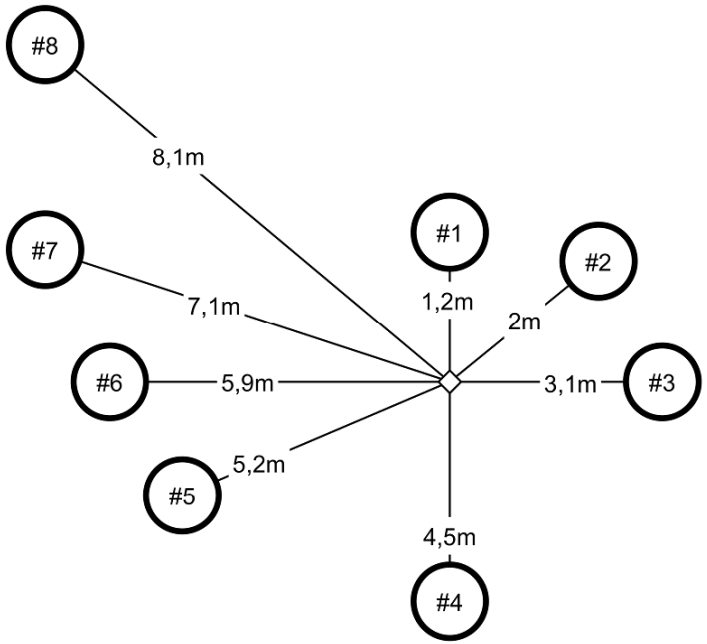
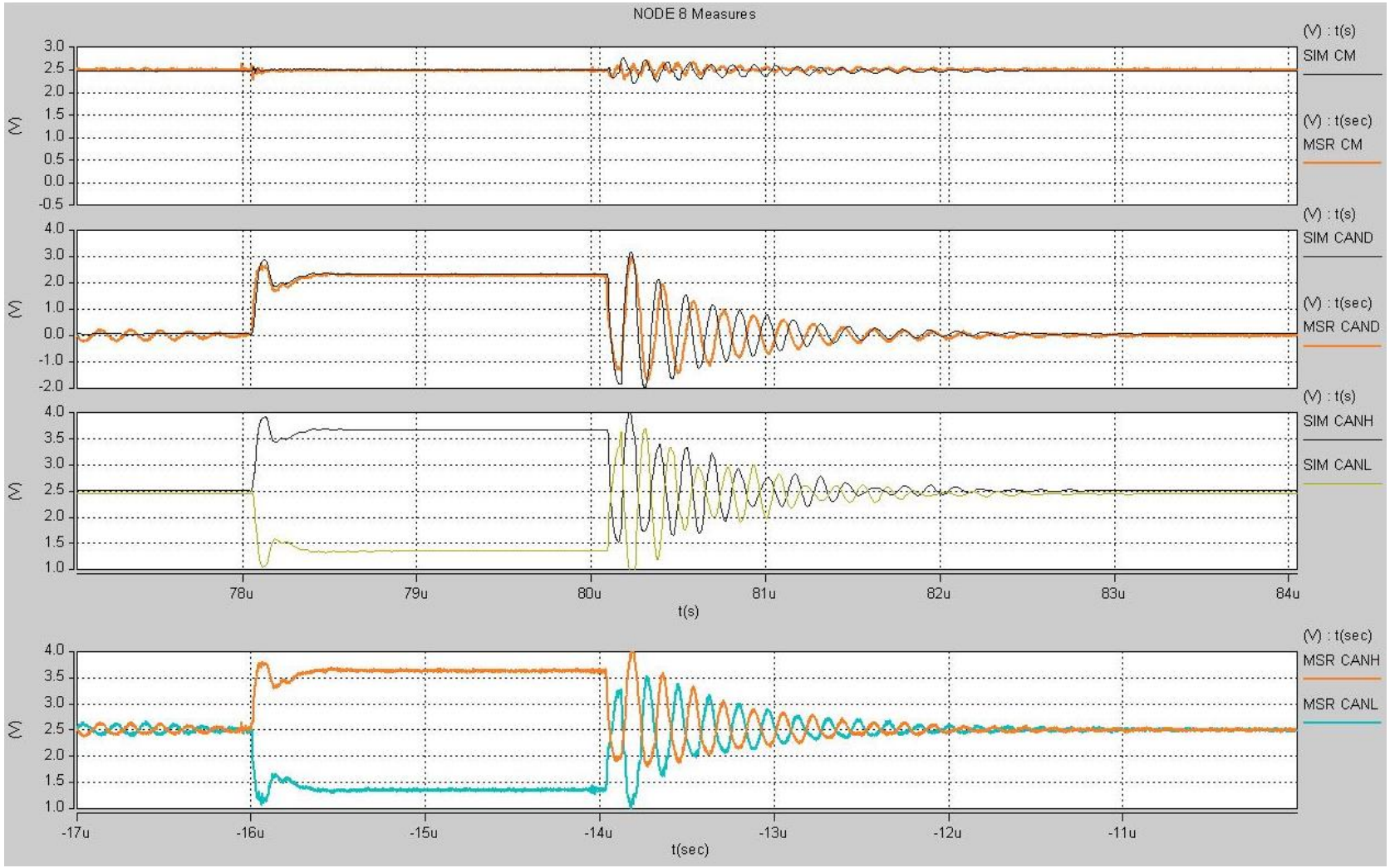
Model development

Topology verification



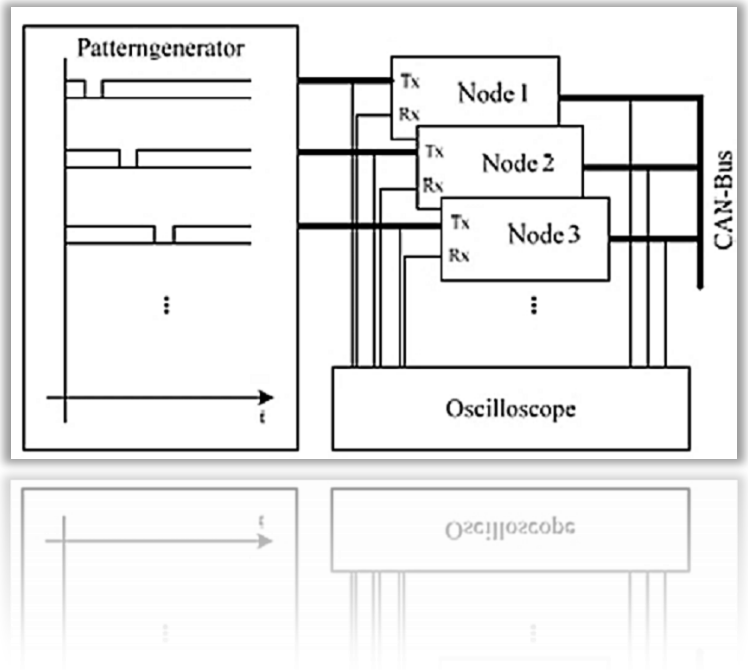
Topology validation – Model development



Topology validation – Stimulus signals (1/2)

Round robin communication

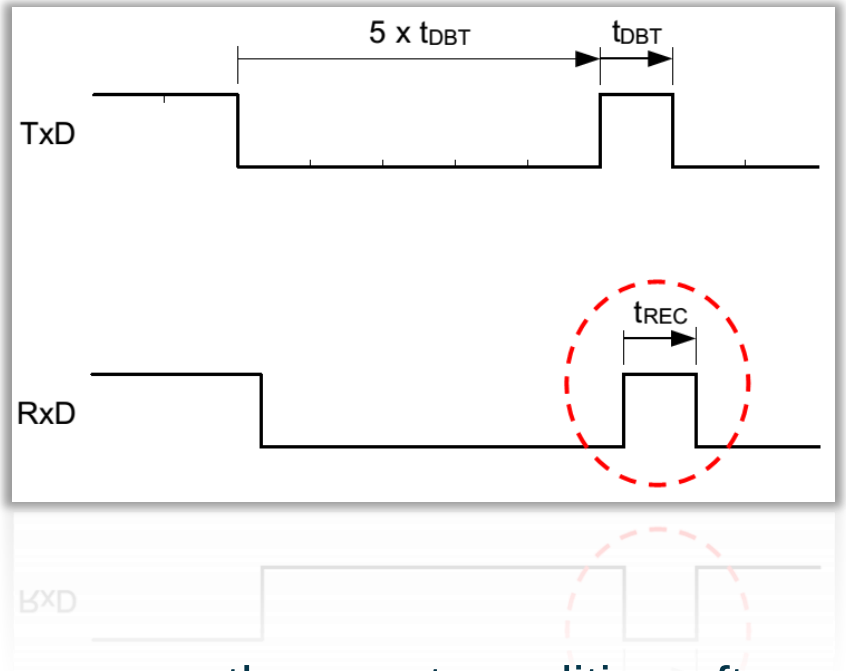
- [Pattern generator] creates a digital input signal to the TXD pin of each transceiver with the required data rate



Topology validation – Stimulus signals (2/2)

Pattern applied to each node

A typical scenario is used when 5 dominant bits are followed by a unique recessive bit



This combination assures the worst condition after charging/discharging the capacitances

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Validation criteria – Clock tolerance, safe sampling

Clock tolerance

Though this rules concentrate on the bit timing only and do not involve topology effects, clock settings must respect the rules defined in "*Robustness of a CAN FD Bus System – About Oscillator Tolerance and Edge Deviations*" by Dr. Arthur Mutter

In special, we consider the clock tolerance as df:

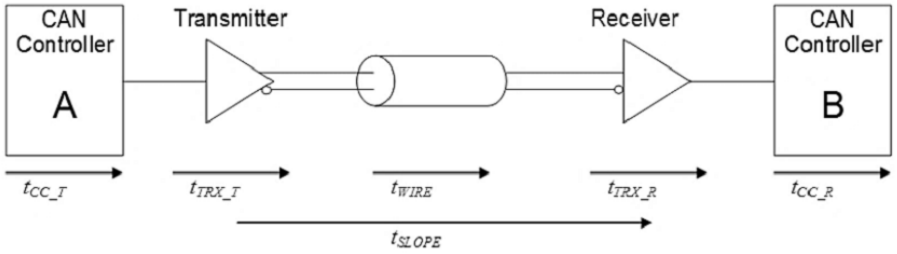
$$(1 - df) < \frac{f_{CAN}}{f_{nom}} < (1 + df)$$

Safe sampling

Focused on the different propagation delays for a dominant to recessive edge and vice versa.

"The symmetry becomes more important with the increasing of the baud rate"

Validation criteria – Safe sampling analysis (1/4)



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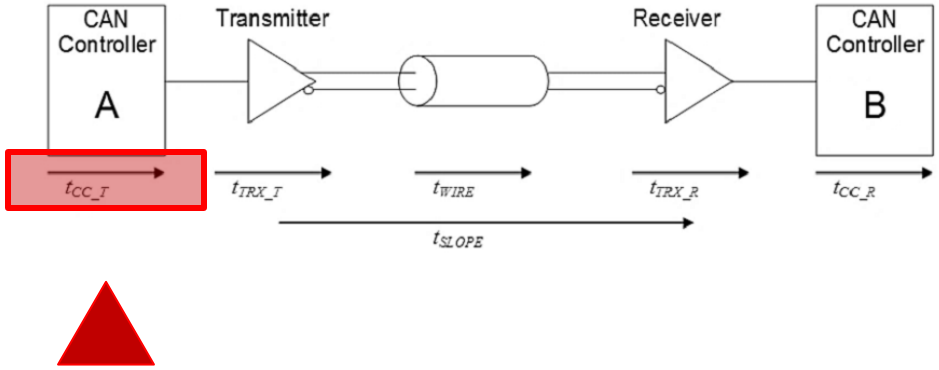

- t_{CC_T} CAN controller delay on the transmitter side
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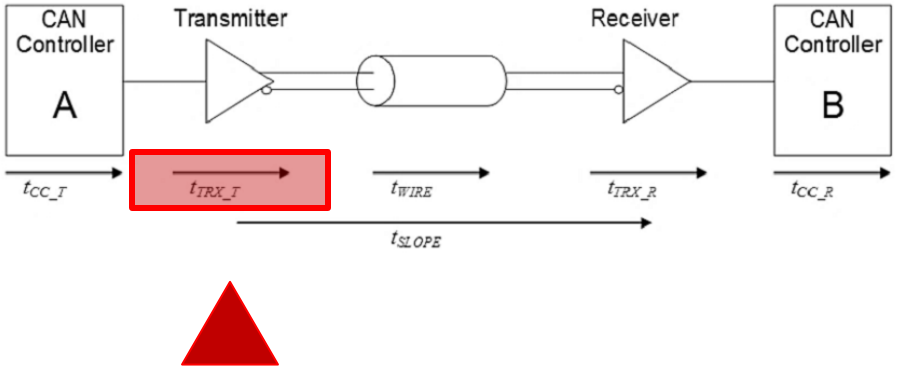
Validation criteria – Safe sampling analysis (1/4)



- t_{CC_T} CAN controller delay on the transmitter side
- t_{TRX_T} Transceiver delay on the transmitter side
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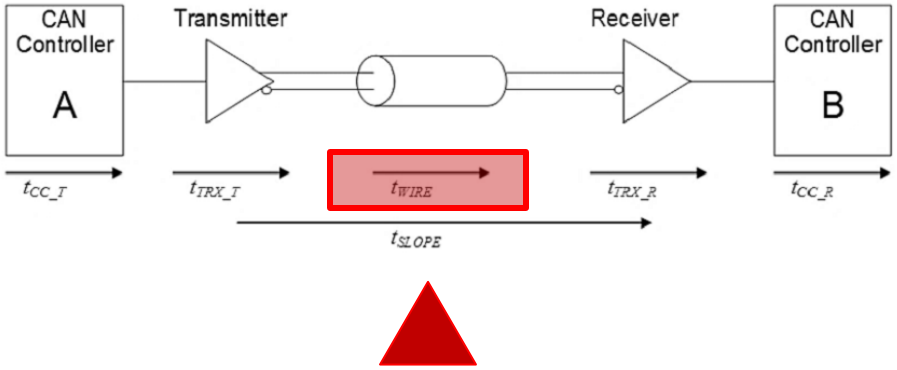

- t_{CC_T} CAN controller delay on the transmitter side
- t_{TRX_T} Transceiver delay on the transmitter side
- t_{WIRE} Wire delays
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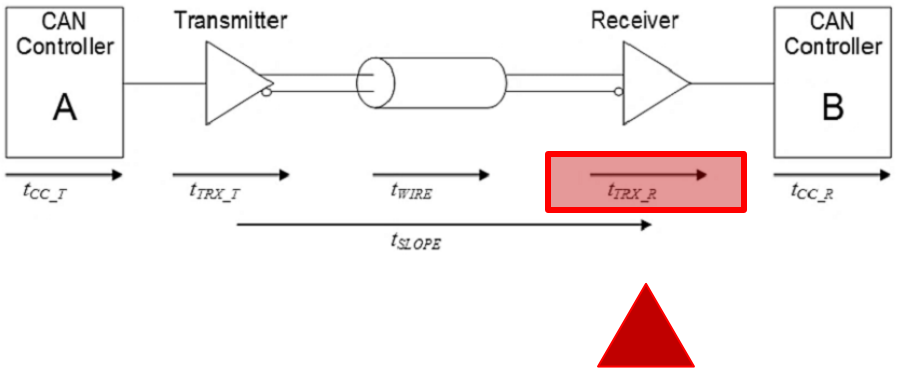
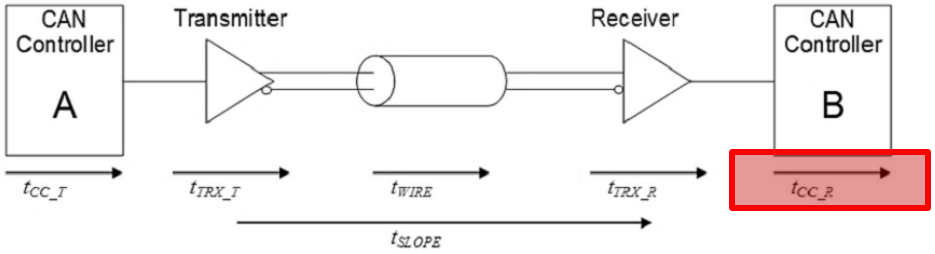


- t_{CC_T} CAN controller delay on the transmitter side
- t_{TRX_T} Transceiver delay on the transmitter side
- t_{WIRE} Wire delays
- t_{TRX_R} Transceiver delay on the receiver side
-

Validation criteria – Safe sampling analysis (1/4)



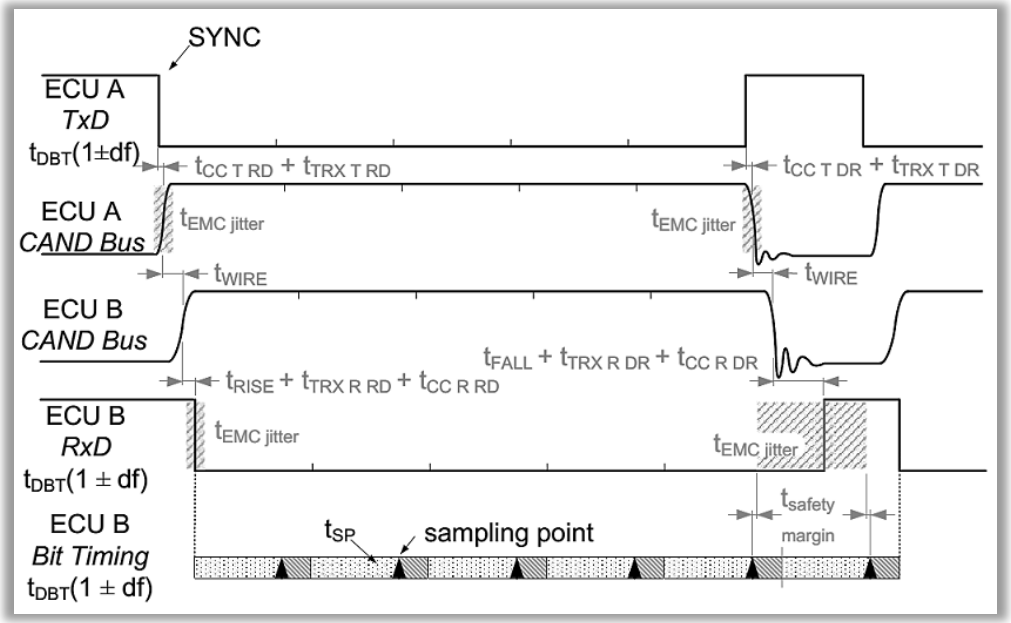
- t_{CC_T} CAN controller delay on the transmitter side
- t_{TRX_T} Transceiver delay on the transmitter side
- t_{WIRE} Wire delays
- t_{TRX_R} Transceiver delay on the receiver side
- t_{CC_R} CAN controller delay on the receiver side

Validation criteria – Safe sampling analysis (2/4)

We consider t_{REC} as:

$$t_{REC} = t_{BIT_D} - \left(t_{TRX\_T_{DR}} - t_{TRX\_T_{RD}}\right) - \left(t_{TRX\_R_{DR}} - t_{TRX\_R_{RD}}\right) - \left(t_{DR} - t_{RD}\right)$$

- t_{REC}: Measured recessive time
- t_{BIT_D}: The time of a bit in data phase
- TRX: Transceiver delay
- T: Transmitting side
- R: Receiving side
- DR: Dominant to recessive edge ($t_{WIRE} + t_{FALL}$)
- RD: Recessive to dominant edge ($t_{WIRE} + t_{RISE}$)



Validation criteria – Safe sampling analysis (3/4)

A safety margin **before** and **after** the sampling point shall be considered

Sampling point - 1st Safety margin

Can be considered as the minimal distance between the sample point and the received edge at the beginning of the ideal bit and

Sampling point - 2nd Safety margin

Minimal distance between the received edge at the end of the ideal bit and the sample point

Validation criteria – Safe sampling analysis (4/4)

For Robustness, following inequalities must be satisfied

– *Supposing that node A is **faster** than node B*

$$t_{REC} < t_{BIT_D} + t_{SP(df_{B+})} + t_{CC} - t_{CLK} - t_{SM}$$

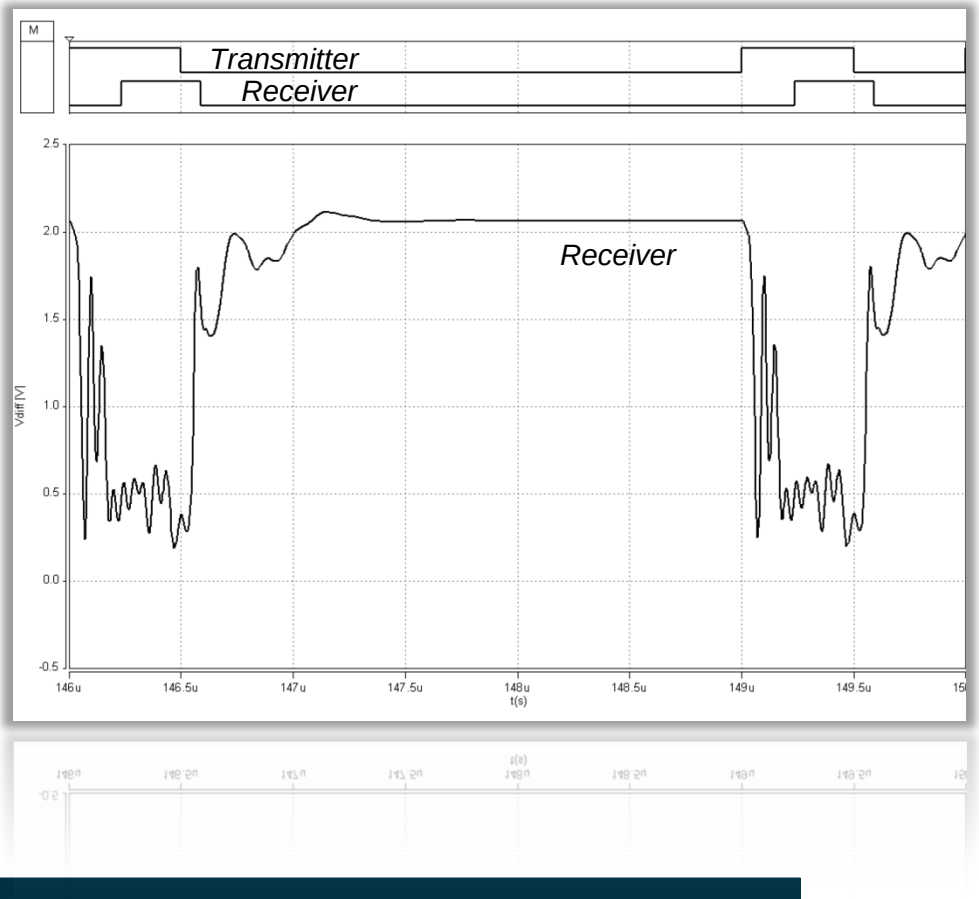
– *Supposing that node A is **slower** than node B*

$$t_{REC} > t_{SP(df_{B-})} + t_{CC} + t_{CLK} + t_{SM}$$

t_{BIT_D}:	The time of a bit in data phase
t_{SM}:	Safety margin including factors as EMC jitter
t_{SP}:	Sample point time within a bit
$df_{B+/-}$:	Index to indicate that the frequency is deviated due to clock deviation
t_{CC} :	Controller processing time
t_{CLK} :	Clock tolerance influence

Validation criteria – Example with t_{REC} too small

Bit time = 500 [ns]

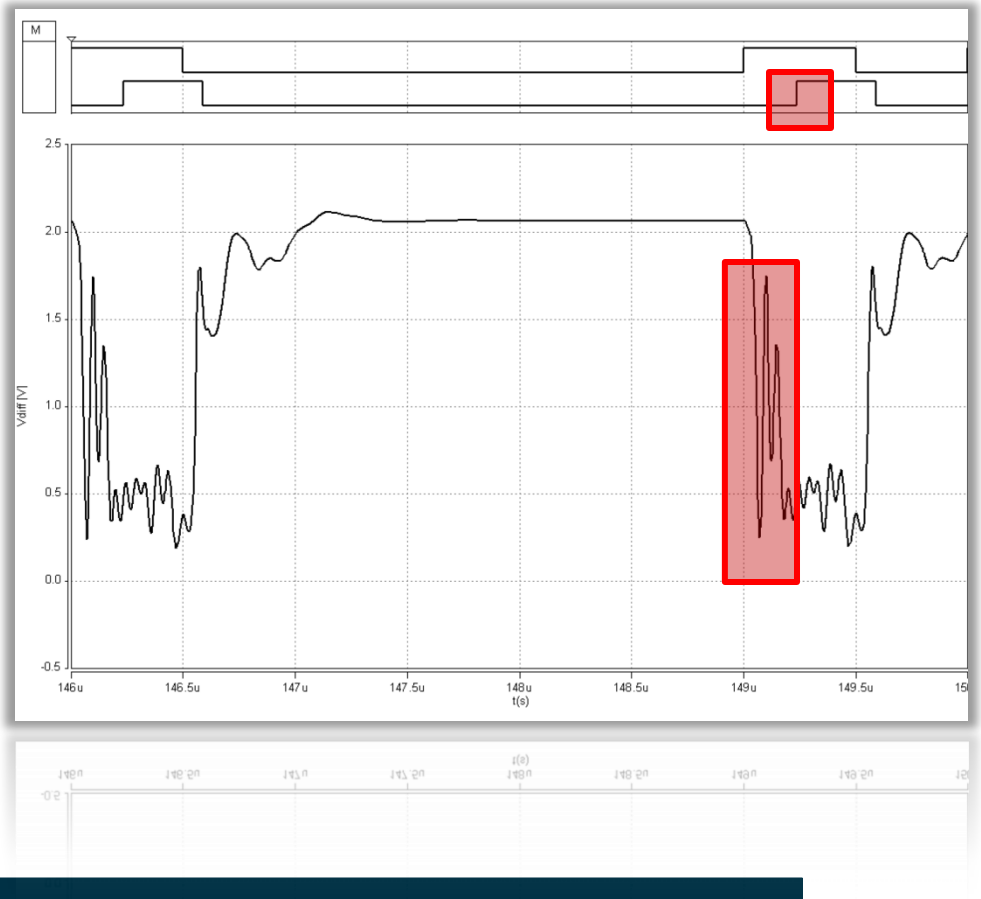


Validation criteria – Example with t_{REC} too small

Bit time = 500 [ns]

Measured value = 179 [ns], thus the minimum is not satisfied.

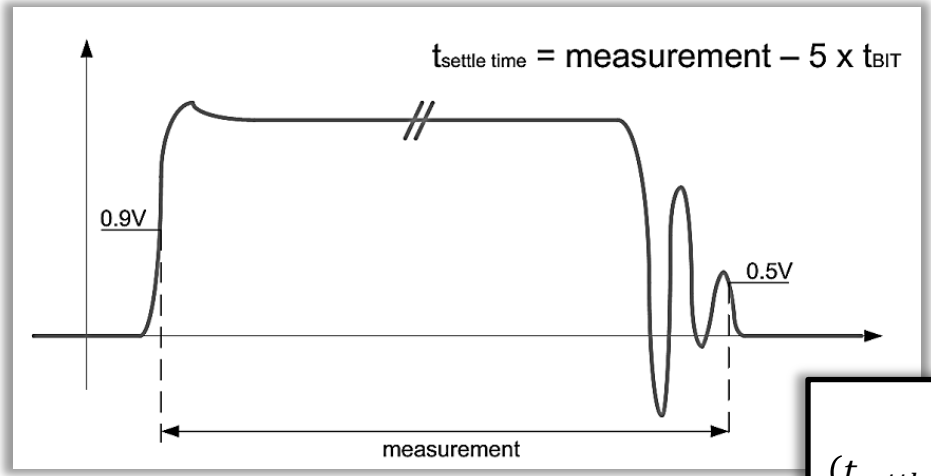
This is reported as a **FAIL** condition for this topology. The same is applied if the recessive time results are too large.



Validation criteria – Settle time

Settle time can be measured in two different approaches

- Edge oriented measurement - Falling time of the signal from the higher threshold to the lower threshold
- Bit oriented measurement - Same as above but including the 5 dominant bits before changing to recessive state



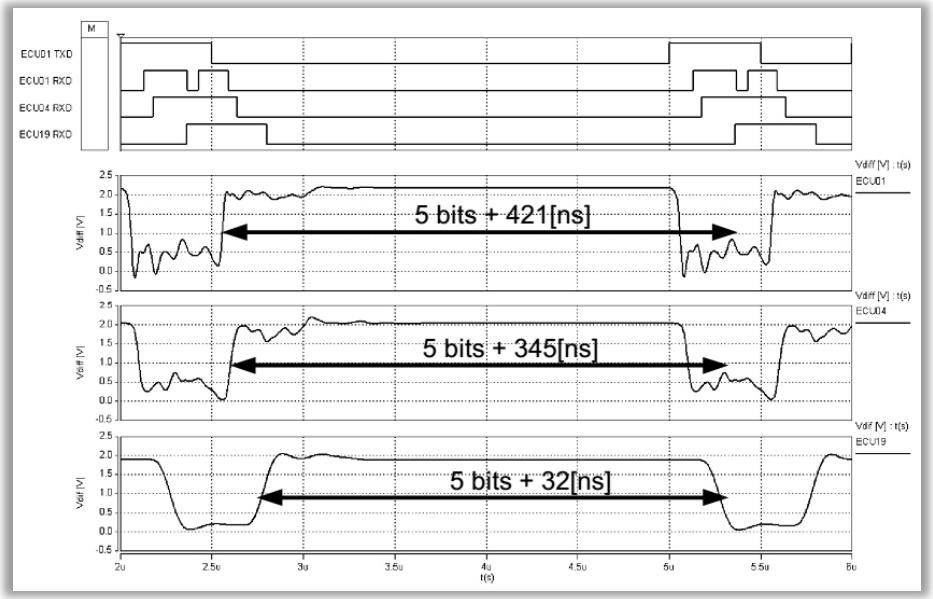
$$\frac{(t_{settle} - 5 * t_{BIT})}{t_{BIT}} \begin{cases} > SP_{\%} \rightarrow not\ ok \\ > 50\%\ and < SP_{\%} \rightarrow warning \\ < 50\% \rightarrow ok \end{cases}$$

Validation criteria – Settle time example

3 different verdicts are met in this example

Table 1: Example of simulation outputs

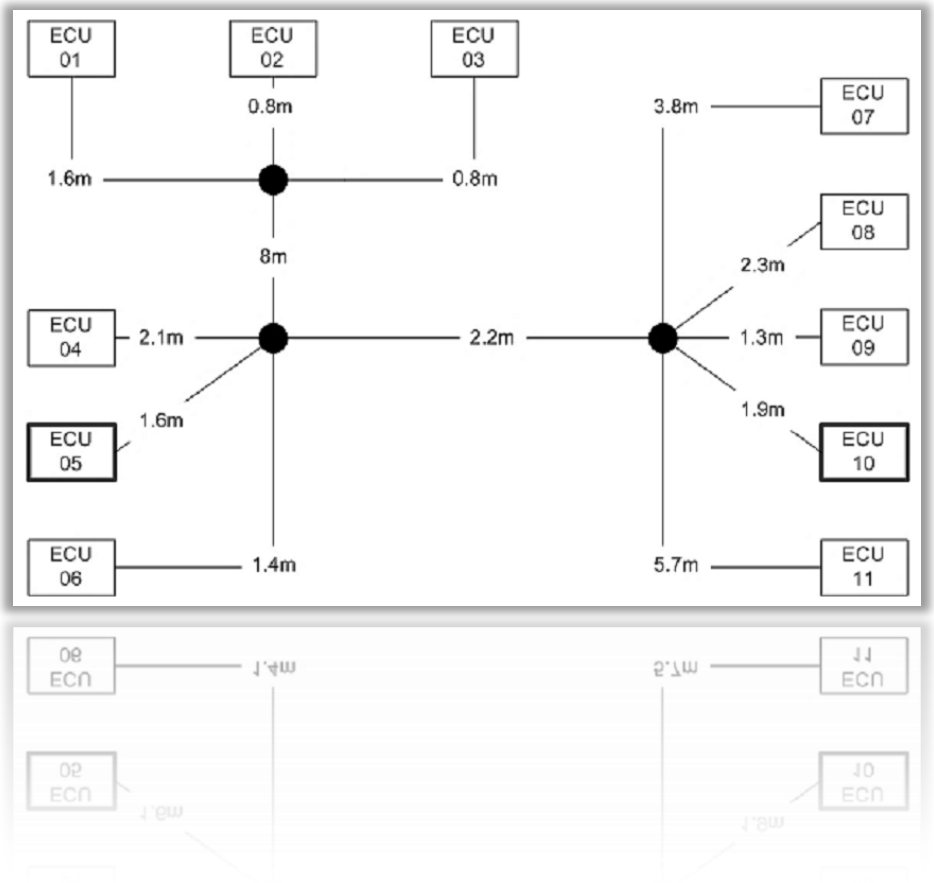
TX node	RX node	Measure	Limit	Verdict
ECU_1	ECU_1	421 [ns]	400 [ns]	FAIL
ECU_1	ECU_4	345 [ns]		WARN.
ECU_1	ECU_{19}	32 [ns]		PASS



Validation criteria – Confidence level (1/4)

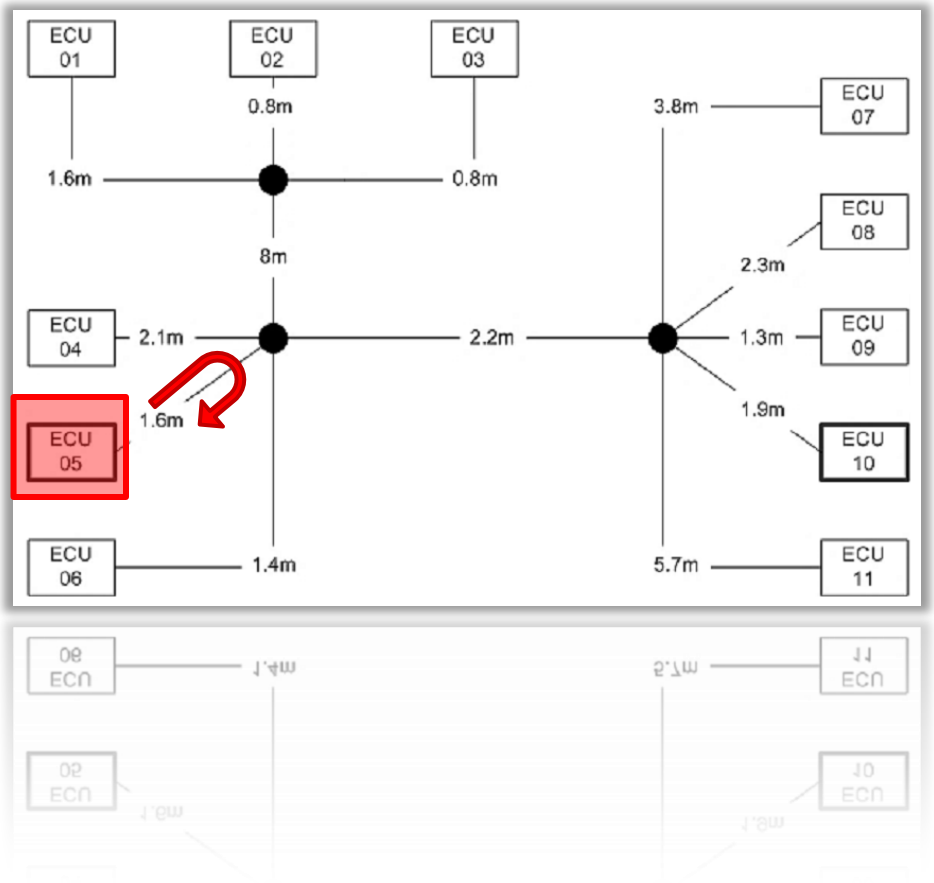
11 Nodes, 2 of them with low resistance termination

3 passive stars

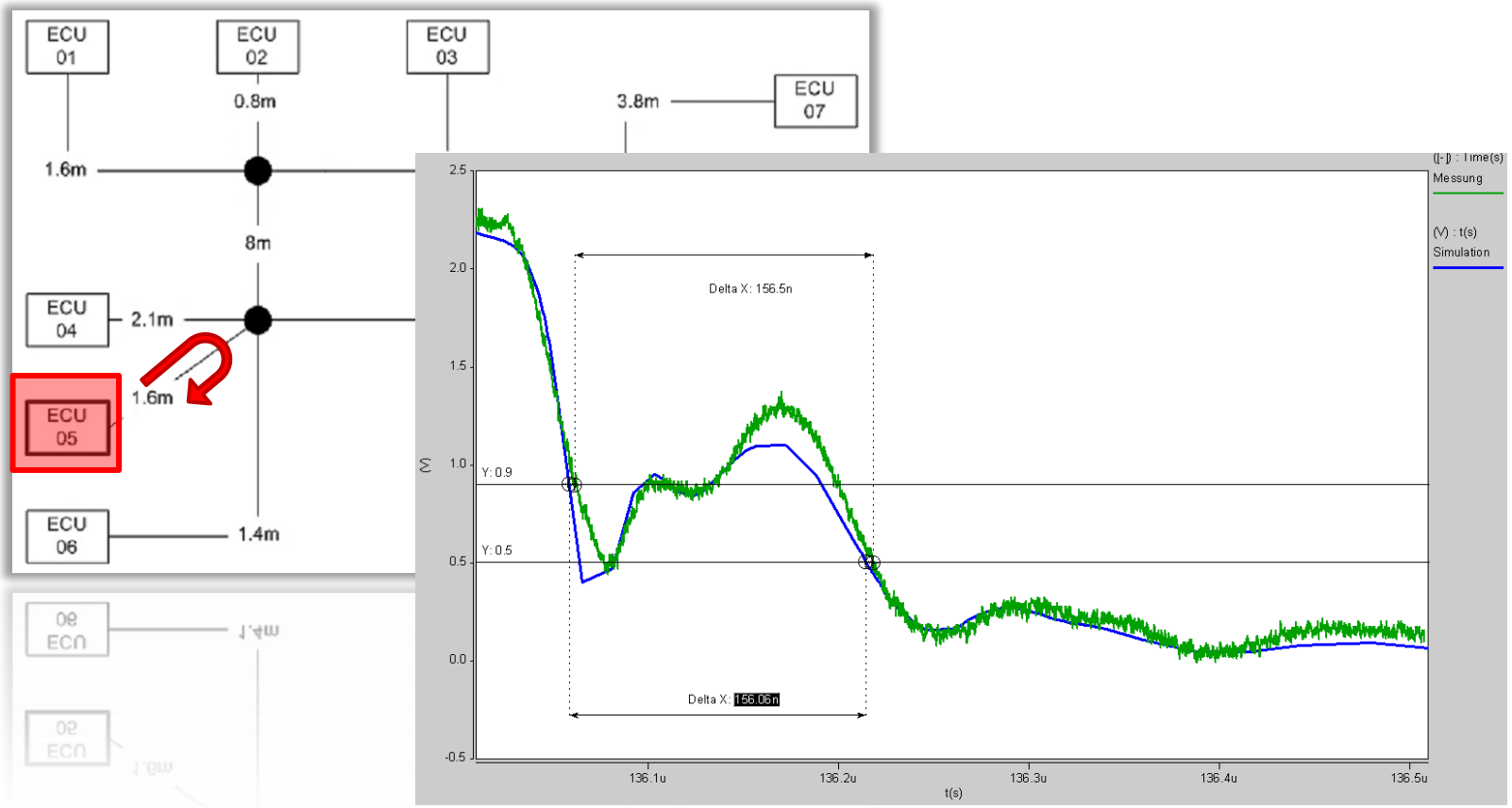


Validation criteria – Confidence level (2/4)

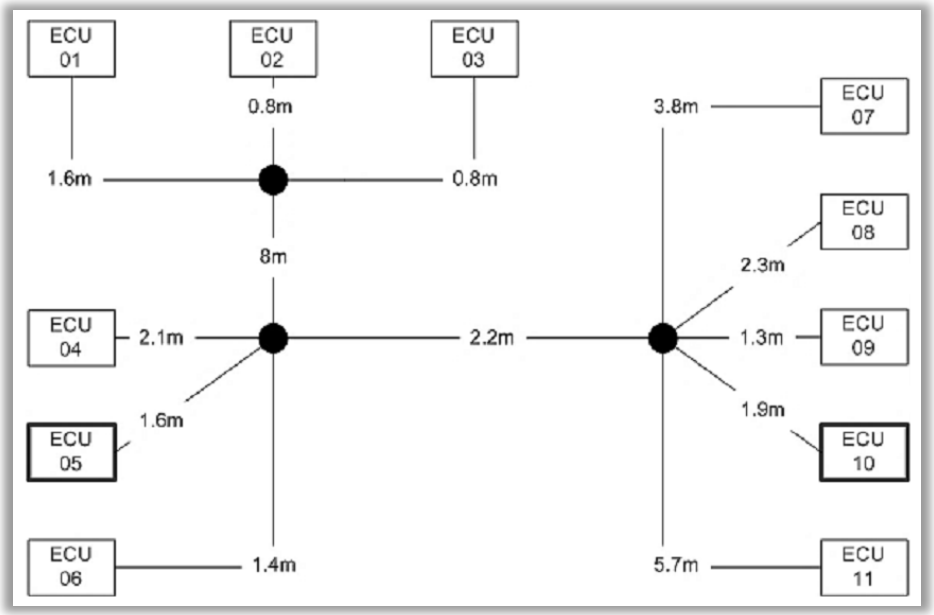
Settle time example



Validation criteria – Confidence level (3/4)



Validation criteria – Confidence level (4/4)



Baud rate [Mb/s]	Simulation	Measurement
0.5	PASS	PASS
1	PASS	PASS
2	PASS[1]	PASS[1]
3	FAIL	FAIL
4	FAIL	FAIL
5	FAIL	FAIL

1. Only with optional TDC

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Need for automatization

- Todays implementations demand automatization
- Each topology is evaluated independently
- Example:
  -
  -
  -
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Need for automatization

- **Nowadays implementations demand automatization**
- **Each topology is evaluated independently**
- **Example:**
  - 11 Nodes (n=11)
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$$n^2[signals]$$

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- **Nowadays implementations demand automatization**
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- **Example:**
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  - 4 edges (Transmitter/Receiver, D2R and R2D)
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$$n^2[signals]\ 4[edges]$$

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- **Example:**
  - 11 Nodes (n=11)
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  - Test at 2Mb/s and at 5Mb/s
  -

$$n^2[signals] \cdot 4[edges] \cdot 2[freq]$$

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- **Example:**
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$$n^2[signals] \,.\, 4[edges] \,.\, 2[freq] \,.\, 3[temp]$$

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$$n^2[signals] \,.\, 4[edges] \,.\, 2[freq] \,.\, 3[temp] = 2904\ measurements!$$

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$$n^2[signals].4[edges].2[freq].3[temp] = 2904\ measurements!$$

Keep counting, we must analyze also the arbitration phase…

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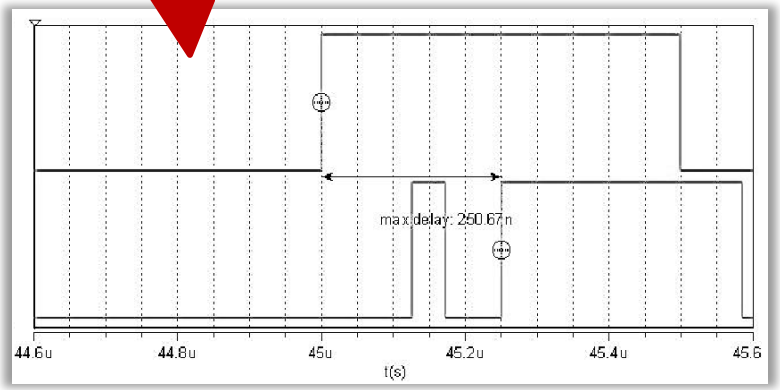
$$n^2[signals].4[edges].2[freq].3[temp] = 2904\ measurements!$$

Keep counting, we must analyze also the arbitration phase…

What about the human error? Automatization gives quality as well

Need for automatization

What happens after measurements? Should we adjust the topology?



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Conclusion

CAN FD means higher data rate and even larger payloads

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CAN FD means higher data rate and even larger payloads

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CAN FD means higher data rate and even larger payloads

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- **The most important factor for higher frequencies is asymmetry and simulation is an excellent tool to evaluate it**
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Conclusion

CAN FD means higher data rate and even larger payloads

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- **The most important factor for higher frequencies is asymmetry and simulation is an excellent tool to evaluate it**
- **Not only typical signals can be analyzed but those affected by tolerances and specified ranges as well**
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Conclusion

CAN FD means higher data rate and even larger payloads

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- The most important factor for higher frequencies is asymmetry and simulation is an excellent tool to evaluate it
- Not only typical signals can be analyzed but those affected by tolerances and specified ranges as well
- Automatization is what makes simulation an effective way in the Topology analysis
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Conclusion

CAN FD means higher data rate and even larger payloads

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- The most important factor for higher frequencies is asymmetry and simulation is an excellent tool to evaluate it
- Not only typical signals can be analyzed but those affected by tolerances and specified ranges as well
- Automatization is what makes simulation an effective way in the Topology analysis
- Automatization + Simulation gives a extended focus to designers

Thank you for your attention!

What can we test for you?

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