Model Conformance Test Specification

V 1.1

Document History

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1 Introduction

1.1 Abstract

The permanent increasing demand of electronic systems and their networking, especially in the automotive and aircraft industry leads to very complex distributed systems built up from an increasing amount of vendors, semiconductors or OEMs. Complex distributed systems are hard and expensive to test and verify and have a negative affect on the time to market. A solution for this is modelling and simulation of these systems / topologies.

Real devices of a distributed system are checked against conformance test specifications to verify the desired operational behaviour. So there is a need for a model conformance test specification. The goal of model conformance testing is now, to ensure defined behaviour in investigations of these distributed systems / topologies and intend to reduce development costs and time to market and finally investigate the systems at worst case scenarios, which can't be met under normal testing circumstances. Another aspect of the model conformance test is to check for the interoperability of the different models from different suppliers regarding the interchangeability of the models within the test environments.

1.2 Aim

The Methods for this conformance test lead to the checking of the model behaviour against underlying protocol-specific transceiver specifications [1], data sheets, GIFT requirements and comparing the model behaviour against real device behaviour.

Further this specification is based on [2]. That means, it is restricted to highspeed-CAN transceivers only.

1.3 Structure

This document is organized into:

- the definition set of the test suite, defining constraints for the simulation process and test reports,
- the test description, forming the basic internals of each single test,
- the test cases, denoting all of the investigation types which are desired at the conformance test

1.4 Terms and Abbreviations

Term / Abbreviation	Meaning
OEM	Original Equipment Manufacturer
CAN	Controller Area Network
PCO	Points of Control and Observation
output level	voltage level at analogue and logical level at digital pins/ports

2 Test Suite

This chapter describes the requirements at the simulation process (with the used simulation algorithms and parameter setups) up to the point of a test report.

The test suite shall execute all test cases specified in chapter 4. However, this specification does not prescribe how the test suite has to be implemented in detail. The only restriction to the test suite is to have a summarized document presenting the correct response of each executed test case afterwards. Which type of document has to be created, is currently up to the customer.

2.1 Simulation Algorithms

The test suite with all of the test cases specified in chapter 4 has to be executed using the Newton-Raphson analog solver algorithm. The Newton-Raphson method is the standard numerical algorithm to solve nonlinear equations and systems of equations. It is an approximation algorithm for finding the roots of a function. Iterations of this method lead to more accurate results. A fix amount of iterations does not lead to identical accuracy in different cases or equations. Therefore the numerical accuracy has to be restricted to confine the error of the results – see next section.

2.2 Simulation Parameters

The goal behind defining limits for the simulation of the test suite is on the one hand, to deal with different simulation environments (with their specific simulation configuration capabilities) which can be used for test executions. On the other hand it aims at keeping the simulation results reproducible and comparable between different simulation runs at either between different simulation environments or at a single simulation environment.

The test suite has to be run with the following specific simulation parameters:

- overall error constraint value for simulation accuracy at 0.0005 (the value is actually based on simulation experience regarding simulation stability and accurate results at reasonable simulation run times)
- a fixed time stepping, with a maximum value of 250ps. Smaller values are possible to recognize ringing.
- no additional nor non common optimisation functionalities. That does not mean, that the test suite cannot run at specific non common optimisations of the simulation

Other simulation parameters not mentioned above have to remain at their default value and may not be altered due to different configuration sets at different simulation environments. The settings of these parameters have to be documented in the test report.

2.3 Test Suite Environment

With the Test Suite, test cases are executed and in the process, digital or analogue values being measured. To reach a certain level of comparability to real device measurements, all probes (no matter how they are implemented) measuring the analogue values have to reflect real probe behaviour with some level of abstraction. That means, input impedances (input resistance, input capacitance) of the probe models shall be implemented / simulated too.

3 Test Description

This chapter takes the detailed description, partitioning and grouping of the tests into account and therefore handles the basic behaviour of every test case and introduces a kind of a system operational vector space to define the limits and variations of each test case.

The general description of this specification introduces generic constants. These are highlighted throughout this document in a ***red*** color. Their values are stated in a table in the appendix of this document.

Pin names as specified in the document of the requirements on transceiver simulation models are highlighted throughout this document in a ***green*** color.

3.1 Basic Behaviour

3.1.1 Handling of different Functionalities

In the current revision of this specification, all of the current test cases are based on repeatedly found data context in an assortment of datasheets of CAN highspeed transceivers. But in fact, datasheets and their content may differ from each other. To handle this, the following behaviours are defined:

- If a transceiver implementation does not support some additional functionality (e.g. wake capabilities), the corresponding tests don't need to be executed. If executed, an info notice shall be documented in the test report with a description of the missing functionality.
- If a datasheet contains no values at specific data context (e.g. missing typical voltage), the corresponding test case for this specific value don't need to be executed. If executed, an info notice shall be documented in the test report with a description of the missing data value in the datasheet.

Furthermore it shall be clear that this test specification shall follow the requirements of the transceiver simulation model specification. Therefore each test case has at maximum up to three variants dealing with different implementation levels of the transceiver models (see chapter 3.6 in [2]).

3.1.2 Test Topology

The test topology can vary as well as the stimuli and the points of control and observation (PCO) in the various test cases. Which different kinds of test topologies and PCOs are needed for specific test cases is summarized as the System Operational Vector Space in the next chapter (3.2) and at the specific test case descriptions in chapter 4.

In order to investigate the transceivers in network topologies, sufficient transmission line models are required. Actually, there is no standardized transmission line model. Therefore the specific transmission line model provided by the used simulation environment has to be applied and its characteristics being documented in the test report.

3.2 System Operational Vector Space

The System Operational Vector Space (SOVS) defines the configuration set for all test case regarding

- the type of circuit,
- the type of abstract temperature modelling parameter,
- how the communication is organized and held between all of the transceivers in the test circuit,
- the type of the transceiver operational modes,
- the type of ground shift and
- different bus failure injections.

At specific test cases, parts of the configuration vector are to be varied, see below.

Circuit Configuration	constant
Parameter Set	variable
Communication	variable
Operating Mode	variable
Ground Shift	variable
Failure	constant

Figure 1: SOVS Variation

In the following sections, each element of the configuration vector is described in more detail. The configuration values are highlighted with a ***blue*** color.

3.2.1 Circuit Configuration

The test cases can be executed with several kinds of circuit configurations, which are constant during one test case.

At all circuit types, every transceiver model is embedded into an ECU node. All additional circuitry, which is transceiver-specific, goes here. All supplies are ideal without any capacitances the voltages are set to the normal / typical values stated in the corresponding datasheet.

3.2.1.1 Single Transceiver Circuit

This circuit configuration is a single transceiver circuit for thresholds and timing characteristics as specified in the datasheet.
Since the datasheets can differ between suppliers or base types of transceivers, the circuit specified in the datasheet has to be taken as the valid circuit configuration (the data values are guaranteed at this circuit by the supplier).

Configuration Value
single_trx

3.2.1.2 Multi Transceiver Circuit

This circuit configuration is a multinode transceiver circuit in a homogenous passive star environment with a total of 8 different stubs (see Figure 2). The stub lengths are defined in the table below Figure 2.

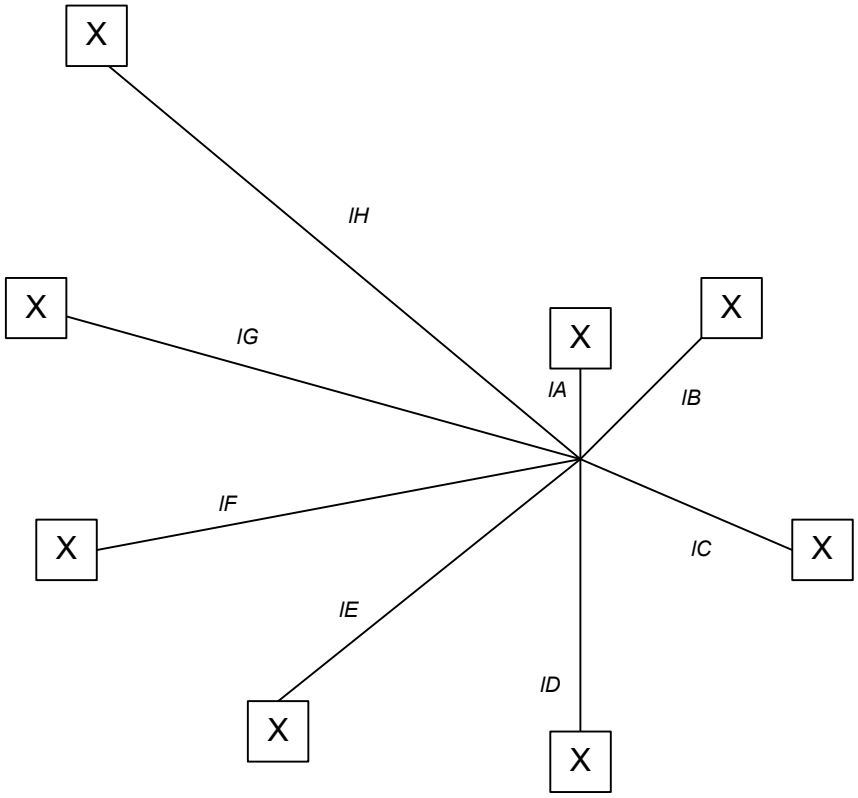


Figure 2: Star Topology with different stub lengths and same transceiver at every node

Stub Name	Length Value (metres)
IA	1.2
IB	2.0
IC	3.1
ID	4.5
IE	5.2
IF	5.9
IG	7.1
IH	8.1

The termination of the net is done by a single resistance (***r_star_term***) between the bus lines ***CANH*** and ***CANL*** at the hub. No additional termination circuitry gets applied at each of the transceiver/ECU.

Configuration Value
star_topology

3.2.2 Parameter Set

The parameter set describes the variation of the transceiver in its different behaviours at several abstract defined temperature areas, see [2]. Each test case shall be executed at each of the parameter set values unless specified otherwise.

Configuration Values
low_temp
typical
high_temp

3.2.3 Operating Mode

During a test case the transceiver operates in a specific mode. At test cases for checking static behaviour, the operating mode remains constant during the test case. If a specific test case needs to be run at several operating modes, the test case is executed more than once (regarding the operating mode) with a variation of the operating mode. At test cases for checking dynamic behaviour, the operating mode can vary at a single test case execution. The operating modes are applied at the digital ***OPM0*** and ***OPM1*** transceiver input pins. ***OPM0*** and ***OPM1*** are assumed as the standard identifiers for the mode control pins. If a transceiver implementation differs from this description, it has to be documented by the manufacturer. For detailed descriptions of the operating modes, see [1].

Configuration Values
normal
low_power
mode_semiconductor

If a test case requires a semiconductor- / device-dependent operating mode setup, the generic mode *mode_semiconductor* is used at the test case setup. The semiconductor has to specify in its application note for a device all implemented operating modes to use for the test case using the mode *mode_semiconductor*. More than one device dependent operating mode is allowed to be implemented and tested. The test case shall then be executed for all implemented operating modes of the device. Only *normal* is applicable to “Level 1” models. For the level implementations, see [2].

3.2.4 Communication / Stimuli

At every test case execution, some kind of communication is needed as stimulus at either the microcontroller pins or at the bus pins depending on the specific test case. While actively transmitting a signal form the transmitter input stage (***TxD***) to the bus lines, the operating mode of the transceiver shall be normal mode. Below are all valid stimuli variants, which are constant during one test case execution:

3.2.4.1 Constant Signal at TxD

The constant level means a constant signal level (constant voltage or corresponding logical level) at the transmitter input stage (***TxD***) at the transceiver resulting in a specific bus state (dominant or recessive). It is used during static behaviour investigations, especially for checks regarding voltage levels and current consumption at the bus pins or power supply pins. The exact voltage values for the two logical levels are determined from the datasheet. The time duration of this stimulus is $1^{*}t_{Bit}$.

Configuration Values
tx_const_high
tx_const_low

The *tx_const_high* value shall result in a recessive bus state and the *tx_const_low* value shall result in a dominant bus state, either if it is implemented digital or analogue. If the transceiver models are implemented as “Level 1” (see [2]), the stimulus graphs are the following:

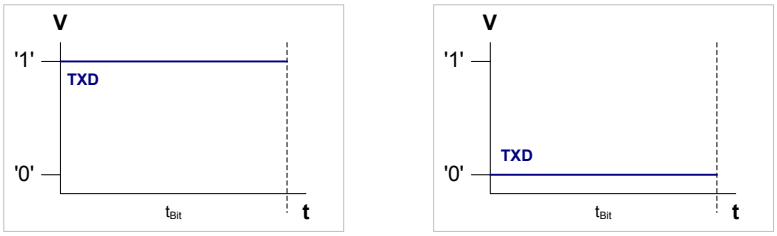


Figure 3: Digital stimulus for *tx_const_high* on the left and *tx_const_low* on the right

If the transceiver models are implemented as “Level 2” or “Level 3” (see [2]), the stimulus graphs are the following:

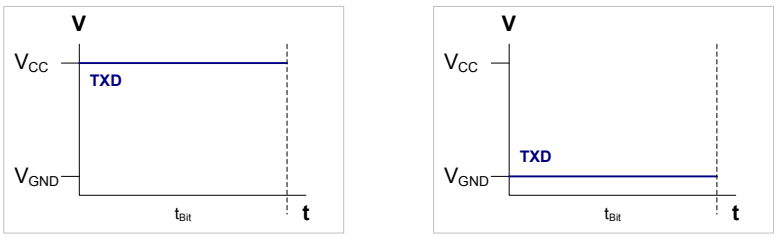


Figure 4: Analog stimulus for *tx_const_high* on the left and *tx_const_low* on the right

3.2.4.2 Single Edge at TxD

The single edge means a single transition at the transmitter input stage (***TxD***) resulting in the corresponding bus state of either a dominant to recessive edge (*tx_rising_edge*) or a recessive to dominant edge (*tx_falling_edge*). This kind of communication is used to check dynamic characteristics such as propagation delays and other timings.

Configuration Values
tx_rising_edge
tx_falling_edge

If not specified otherwise, the dominant and recessive states before and after the transition last 1*t_{Bit} at each. If the transceiver models are implemented as “Level 1” (see [2]), the stimulus graphs are the following:

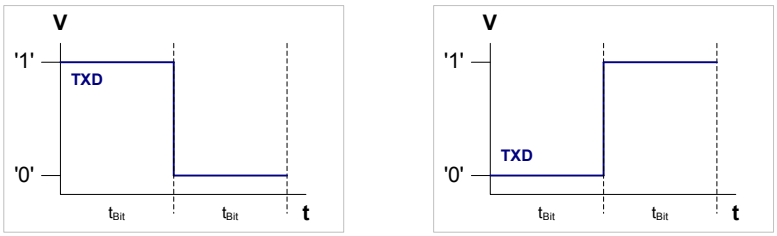


Figure 5: Digital stimulus for *tx_falling_edge* on the left and *tx_rising_edge* on the right

If the transceiver models are implemented as “Level 2” or “Level 3” (see [2]), the stimulus graphs are the following:

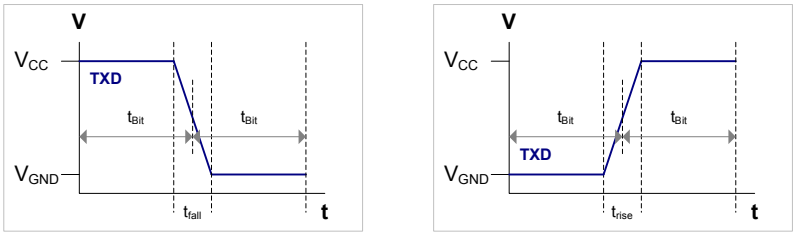


Figure 6: Analog stimulus for *tx_falling_edge* on the left and *tx_rising_edge* on the right

3.2.4.3 Negative Pulse at TxD

The negative pulse is a single bit transmission, that indicates two opposite consecutive single edges at the transmitter input stage (***TxD***) resulting in a recessive to dominant to recessive state change at the bus pins. Each state lasts 1*t_{Bit}

Configuration Values
tx_neg_pulse

If the transceiver models are implemented as “Level 1” (see [2]), the stimulus graphs are the following:

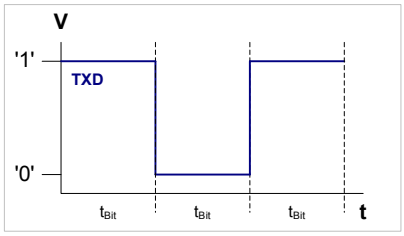


Figure 7: Digital stimulus for *tx_neg_pulse*

If the transceiver models are implemented as “Level 2” or “Level 3” (see [2]), the stimulus graphs are the following:

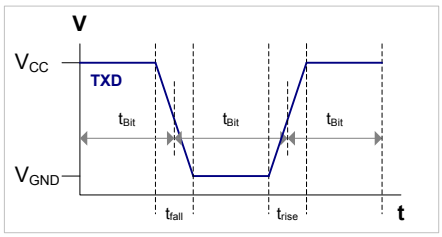


Figure 8: Analog stimulus for *tx_neg_pulse*

3.2.4.4 Current Ramp between INH and V_{BAT}

This stimulus type is used for measuring the high level voltage drop at the ***INH*** pin of the transceiver. Therefore a current source is connected between ***INH*** and V_{BAT} and the current of this source is ramped up starting from I_0 up to the value I_{INH} of the transceiver specific datasheet. At this stimulus, the ***TxD*** pin shall be held in recessive state (*tx_const_high*). The time duration of the stimulus is 1*t_{Bit}. This stimulus is not appicable to “Level 1” models, see [2].

Configuration Values
inh_cur_ramp

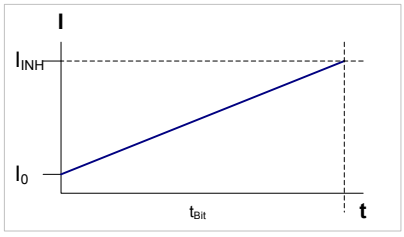


Figure 9: Current ramp

3.2.4.5 Current Source at SPLIT

This stimulus applies a current source at the ***SPLIT*** pin for measuring the Split output voltage according to ISO11898-5, see [1]. This stimulus can not be applied to “Level 1” and “Level 2” models which do not contain a split pin. This refers also to test cases using this stimulus.

Configuration Values
split_cur_iso

3.2.4.6 Dominant Pulse at Bus

The bus dominant pulse sequence applies a recessive to dominant to recessive state change at the bus lines with a time duration of the dominant state at 1*t_{Bit}. The time duration for the recessive states shall be at minimum 1*t_{Bit}, too. The operating mode of the transceiver shall be *receive_only*.

Configuration Values
bus_dom_pulse

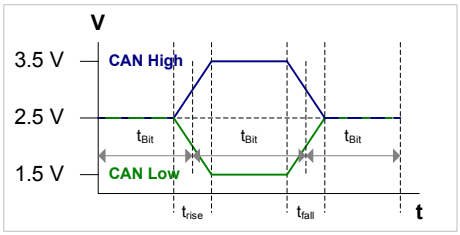


Figure 10: Stimulus graph for the dominant pulse at the bus

3.2.4.7 Receiver Threshold Sequence

The receiver threshold sequence is a stimulus with a slow ramp at the bus pins from recessive to dominant and back to recessive with the maximum differential bus voltage at dominant state taken from [1]. It is used to measure the threshold voltages for the receiver to indicate “crossing points” at switching of logical levels and to measure the hysteresis voltage of the receiver.

Configuration Values
bus_ramp

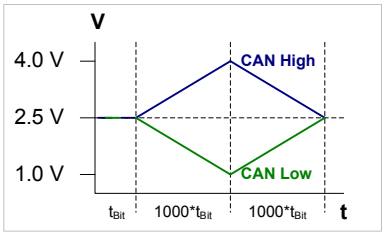


Figure 11: Stimulus graph for the bus ramp at the bus

3.2.4.8 Wake Sequences by Semiconductor

The sequence to wake up a transceiver via bus or pin shall be described by an application note about the stimulus setup for the specific test case using these stimuli provided by the semiconductor. The starting operating mode of the transceiver shall be low power mode. Both of these stimuli can not be applied to “Level 1” models, see [2].

Configuration Values
wbus_semiconductor
wpin_semiconductor

3.2.4.9 Wake Ramp Sequence

The wake ramp sequence applies a stimulus at the wake pin for a local wake-up of the transceiver. The operating mode of the transceiver shall be low power mode. This stimulus can not be applied to “Level 1” models, see [2]. Depending on the device implementation, falling ramps, rising ramps or both are necessary for the operation at the WAKE pin.

Configuration Values
wake_ramp

The *wake_ramp* stimulus can be one of the following figures 12.1, 12.2 or 12.3. For the rising ramps the signal must start at zero volts and ends at battery supply voltage or the maximum allowed voltage according to the datasheet. For the falling ramp the signal starts at battery supply voltage or the maximum allowed voltage according to the datasheet and ends at zero volt. The time duration shall be 100ms.

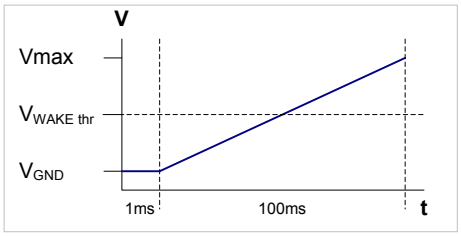


Figure 12.1: Rising Ramp at WAKE pin

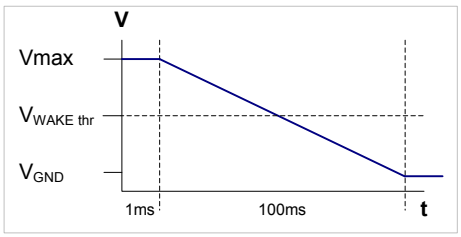


Figure 12.2: Falling Ramp at WAKE pin

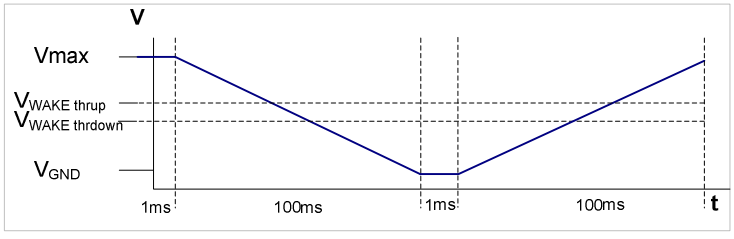


Figure 12.3: Falling and Rising Ramp at WAKE pin

3.2.4.10 Go-to-Sleep Sequence

The go-to-sleep command applies a sequence of state changes at the mode control input pins ***OPM0*** and ***OPM1*** of the transceiver. These state changes depend on the device-dependent possible operating modes the transceiver was before the mode change. The beginning mode is held with a time duration of 1*t_{Bit} and after the go-to-sleep command, the mode is held with a time duration of 100*t_{Bit}. This stimulus can not be applied to “Level 1” models, see [2].

Configuration Values
goto_sleep

3.2.4.11 Round Robin Communication at TxDs

At a multi transceiver topology setup a round robin communication with a single bit transmission can be used. The stimulus is applied at the transmitter input stages (***TxD***) at each transceiver within all topologies descibed in Ch. 3.2.1.2. The sending transceiver is in normal operating mode. While this communication type, every node sends an analog negative pulse, respectively a digital positive pulse, with a time duration of 1*t_{Bit} for each state of the pulse.

Configuration Values
tx_round_robin

If the transceiver models are implemented as “Level 1” (see [2]), the stimulus graphs are the following:

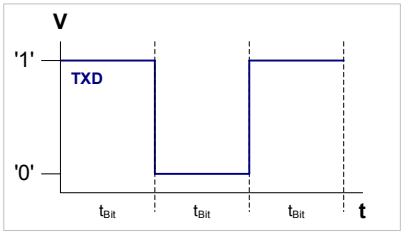


Figure 13: Digital Stimulus Sequence for each sending ECU

If the transceiver models are implemented as “Level 2” or “Level 3” (see [2]), the stimulus graphs are the following:

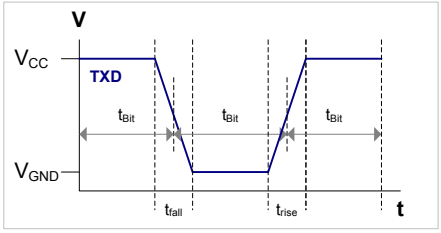


Figure 14: Analog Stimulus Sequence for each sending ECU

3.2.4.12 Two Nodes Communication at TxDs

This communication type is a reduced version of the round robin communication at test cases with the circuit configuration *star_topology*, where only node 1 and node 8 are sending a dominant bit to the bus.

Configuration Values
tx_two_nodes

3.2.5 Ground Shift

The test cases should be executed with several kinds of shifting the ground voltage value, which are constant during one test case:

Configuration Values
none

The configuration value above indicates a ground shift of 0V and therefore being the normal case without ground shift.

3.2.5.1 Static Ground Shift

With a static shift of the ground, the voltage level is shifted within a defined voltage range. The ground shift range is fixed to +5V to -5V. Only the corner cases at +5V and -5V are checked.

Configuration Values
static

A test case will be executed three times (-5V up to +5V in 5V steps) regarding static ground shift variation, where each static ground shift values gets applied at only one test execution.

3.2.5.2 Dynamic Ground Shift

The dynamic variation of ground shift means a variation of the voltage level at one test case execution. For further information of the dynamic ground shift sequence, see chapter 3.4 at [2].

Configuration Values
dynamic

3.2.6 Failure

From a certain point of view, every test case is executed with a specific failure injection to check the behaviour of transceiver at non-normal network conditions. With this, a “no failure” can be treated as just one kind of failure. The failure injection type remains constant during one test case.

3.2.6.1 No Failure

At this failure type, no special failure injection is applied at the bus lines.

Configuration Values
none

3.2.6.2 Loss of Power

At loss of power, the power supplies are set to ground after a normal state.

Configuration Values
loss_power

After the falling edge for the power supply voltage drop is applied, the low power is held with a time duration of 10*t_{Bit}, see figure 15 below.

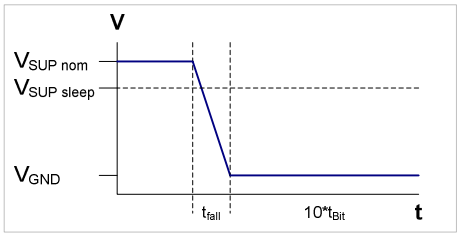


Figure 15: Power Supply Voltage Drop

3.2.6.3 Loss of Ground

At loss of ground, ground is set to the supply voltage level after a normal state.

Configuration Values
loss_ground

After the rising edge at the ***GND*** pin, the high voltage level is held with a time duration of 10*t_{Bit}, see figure 16 below.

Figure 16: Loss of Ground Application

3.2.6.4 Short Circuit

At short circuit failure injection, there are 3 general types of short circuit connections. The first short circuit connection is between ***CANH*** and ***CANL***, the second connects ***CANH*** to either ground or power supply and the third connects ***CANL*** to either ground or power supply (V_{BAT}). The shorts at the bus pins are located directly after any additional circuitry (like termination and stability network) at each stub of the network if present, else directly at the bus pins of the transceiver. Therefore a test case with a short circuit failure injection is going to be executed five times (regarding the short circuit types).

Configuration Values
canh_to_canl
canh_to_gnd
canh_to_pwr
canl_to_gnd
canl_to_pwr

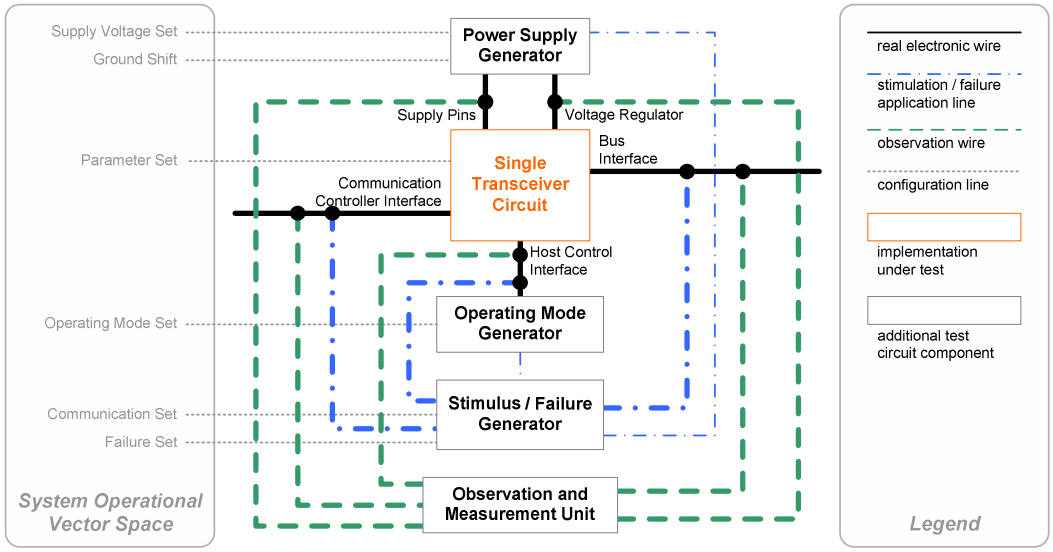
3.2.6.5 Open Wire

At open wire failure injection, there are 2 types of open wire conditions. The first open wire is applied at ***CANH*** and the second is applied to ***CANL***. Open wires at both bus lines at a time won't be considered. Therefore a test case with open wire failure injection is going to be executed two times (regarding the open wire types). The open wire condition is modelled as a high-ohmic resistor with the value ***r_openwire*** and is located directly after any additional circuitry (like termination and stability network) at each stub of the network if present, else directly at the bus pins of the transceiver.

Configuration Values
canh_open
canl_open

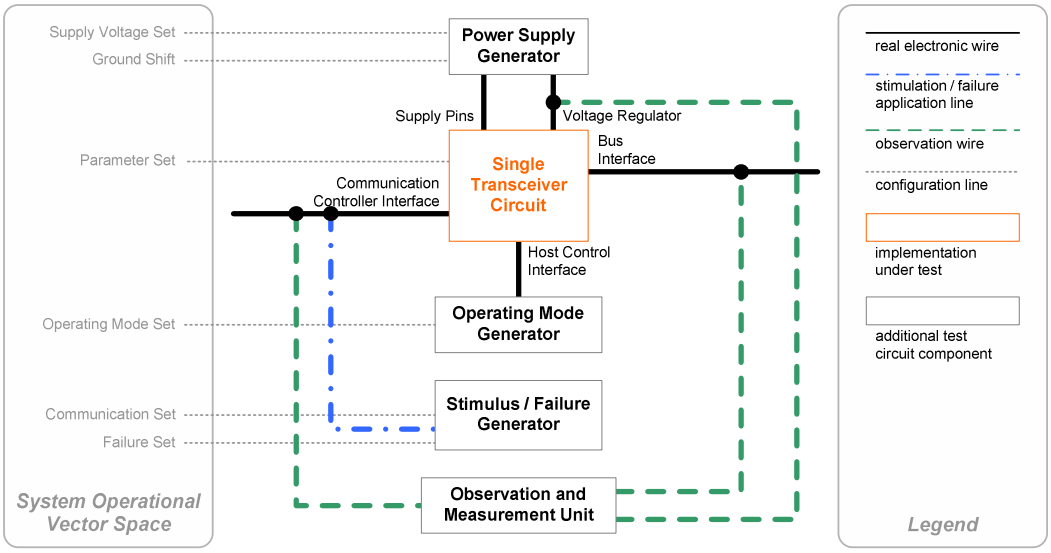
4 Test Cases

In this chapter, all upcoming test cases for the model conformance test are specifed. An example is given below, how every test case description is organized.

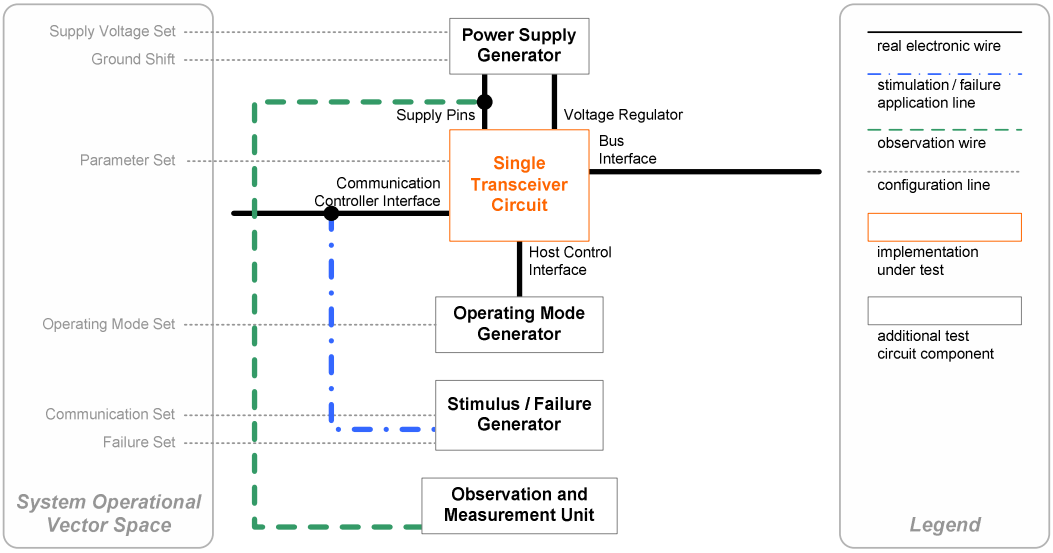
Description	A short description of the purpose of the test case is given here. A bold marked **matching type** of the simulation results is also stated here for clarification. A bold marked **application level** gives information about to which level implementation of the transceiver model the specific test case is applied.
Setup	The SOVS configuration setup for the test circuit is given here. Setup variations are highlighted with ***orange*** color.
Execution	The first note here describes the total sum of test case executions due to setup variations and how many nodes being stimulated to give the test implementer a first impression of time estimation for the specific test case. Optional conditions may also appear in this cell, e.g. only specific communications at specific operating modes. As the third part of the test case execution, the test steps are described dealing with the setup being applied and what is observed and measured at each execution etc. The last part shows a formal picture of the peripheral test case setup with its control and observation points, like the figure below with all possible combination lines. 
Response	In this response cell, a description is given about what is expected as the result, e.g. comparison with real measurements or datasheet values etc.
Reference	This cell links to the chapter in the requirement specification for transceiver simulation models the test case deals with.

4.1 Static Behaviour

4.1.1 Operational Mode State Checks

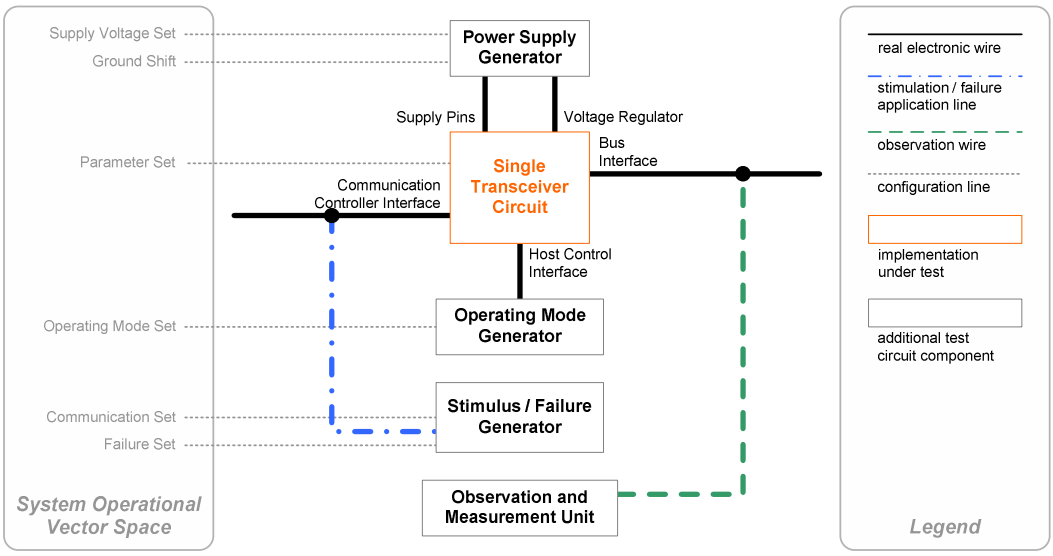
Description	This test shall ensure that the output levels at the transceiver pins *INH*, *RXD*, *SPLIT* (if appicable at the investigated model) and additionally implemented diagnostic outputs (at level 3 model implementations) are fulfilling the datasheet of the real device and follow the requirements of the transceiver model specification. Matching Type: **Datasheet** Application Level: **2, 3**
Setup	Circuit Configuration: *single_trx* Parameter Set: *low_temp* | *typical* | *high_temp* Operating Mode: *normal* | *low_power* | *mode_semiconductor* Communication: *tx_const_high* | *tx_falling_edge* Ground Shift: *none* Failure: *none*
Execution	The variation of the parameter set, operating mode and communication result into a sum of 3 test executions per operating mode (see Conditions below). Conditions: - at low power modes, the communication is *tx_const_high* - at normal modes, the communication is *tx_falling_edge* Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 2 nested parameter variations - at each execution, the output levels are observed at *INH*, *RXD* and *SPLIT* pins and at level 3 models additional diagnostic pins 
Response	The output levels at the *INH*, *RXD* and *SPLIT* pins shall match exactly or lay within the limits of the given values in the corresponding datasheet of the transceiver device. The output level of digital diagnostic output pins of shall indicate no error.
Reference	3.3, 3.4

4.1.2 Power Supply Input Current Consumption

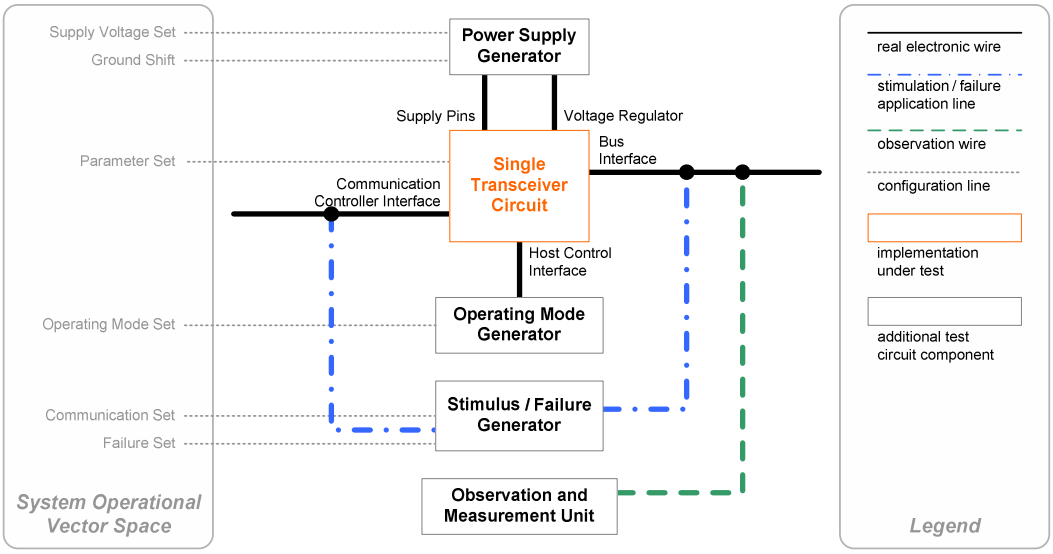
Description	This test shall ensure that the current consumption at the power supply input pin(s) at different transceiver operating modes are fulfilling the datasheet of the real device and follows the requirements of the transceiver model specification. Matching Type: **Datasheet** Application Level: **2, 3**
Setup	System Configuration: *single_trx* Parameter Set: *low_temp* | *typical* | *high_temp* Operating Mode: *normal* | *low_power* | *mode_semiconductor* Communication: *tx_const_high* | *tx_falling_edge* Ground Shift: *none* Failure: *none*
Execution	The variation of the parameter set, operating mode and communication result into a sum of 3 test executions per operating mode (see Conditions below). Conditions: - at low power modes, the communication is *tx_const_high* - at normal power modes, the communication is *tx_falling_edge* Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 2 nested parameter variations - at each execution, the current is observed at the existing power supply input pin(s) of the transceiver 
Response	The input currents at the power supply pin(s) V_{CC} (V_{BAT}, V_{IO}) shall match exactly or lay within the limits of the given values in the corresponding datasheet of the transceiver device.
Reference	3.3, 3.4

4.1.3 Transmitter Stage

4.1.3.1 Transmitter Output Voltages and Currents

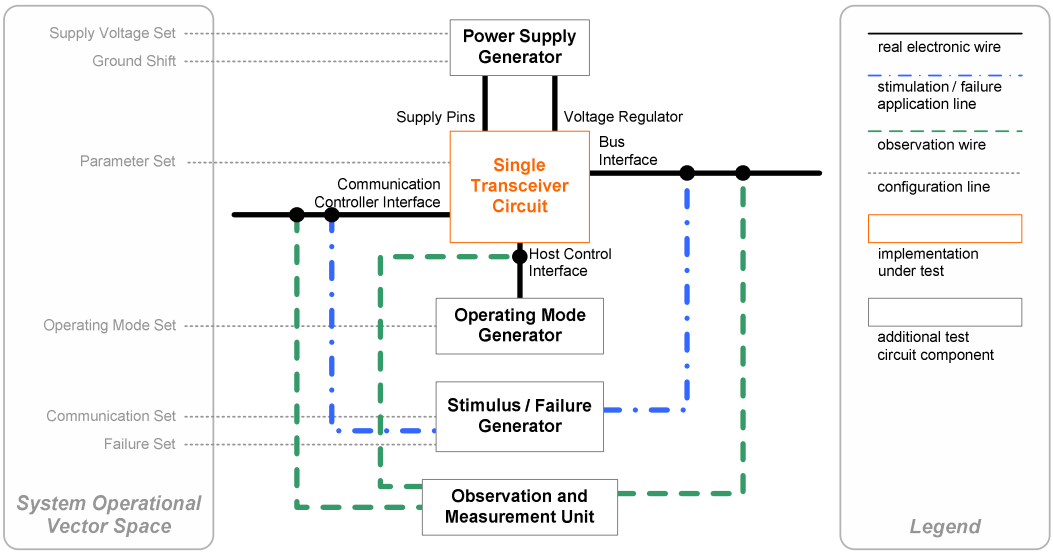
Description	This test shall ensure that the output voltage, output current at and the differential voltage between the bus pins *CANH* and *CANL* at different communication input levels are fulfilling the datasheet of the real device and follows the requirements of the transceiver model specification. Matching Type: **Datasheet** Application Level: **1, 2, 3**
Setup	System Configuration: *single_trx* Parameter Set: *low_temp* | *typical* | *high_temp* Operating Mode: *normal* Communication: *tx_const_high* | *tx_const_low* Ground Shift: *none* Failure: *none*
Execution	The variation of the parameter set and communication result into a total sum of 6 test executions (see Conditions below). Conditions: - at communication type *tx_const_high*, no load at the bus Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 2 nested parameter variations - at each execution, the voltage and current is observed at the bus pins *CANH* / *CANL* and the differential voltage between the bus pins *CANH* and *CANL* of the transceiver 
Response	The output voltage, output current at and the differential voltage between the bus pins *CANH* and *CANL* shall match exactly or lay within the limits of the given values in the corresponding datasheet of the transceiver device.
Reference	3.3, 3.4

4.1.3.2 Transmitter Short Circuit Output Current

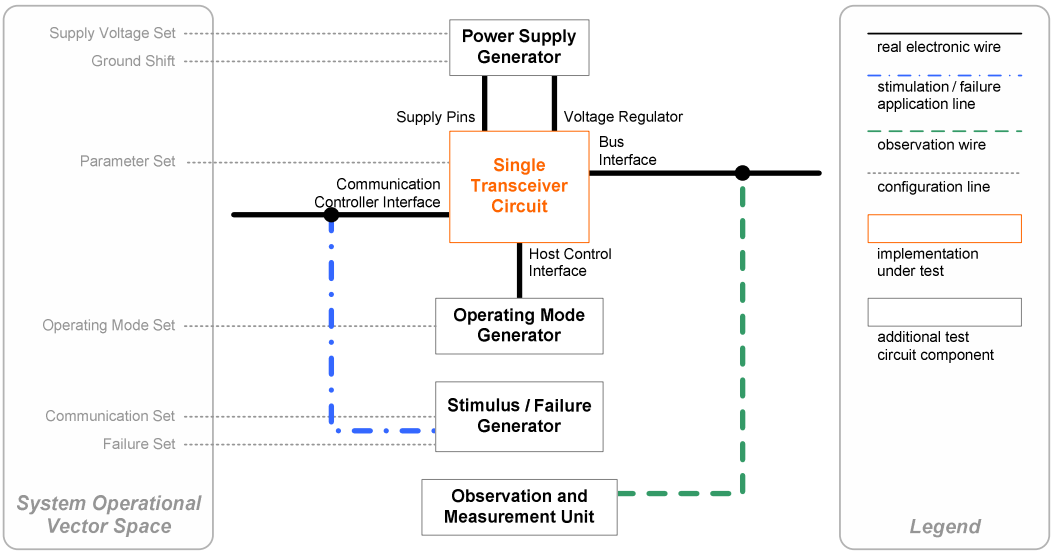
Description	This test shall ensure that the output current consumption at a short circuit condition at the bus lines *CANH* and *CANL* are fulfilling the datasheet of the real device and follows the requirements of the transceiver model specification. Matching Type: **Datasheet** Application Level: **1, 2, 3**
Setup	System Configuration: *single_trx* Parameter Set: *low_temp* | *typical* | *high_temp* Operating Mode: *normal* Communication: *tx_const_low* Ground Shift: *none* Failure: *canh_to_gnd* | *canl_to_pwr*
Execution	The variation of the parameter set and failure result into a total sum of test 6 executions. Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 2 nested parameter variations - at each execution, the current is observed at the shortened bus pin *CANH* or *CANL* of the transceiver 
Response	The output currents at the shortened bus pins *CANH* and *CANL* shall match exactly or lay within the limits of the given values in the corresponding datasheet of the transceiver device.
Reference	3.3, 3.4

4.1.4 Receiver Stage

4.1.4.1 Receiver Differential Threshold and Hysteresis Voltage

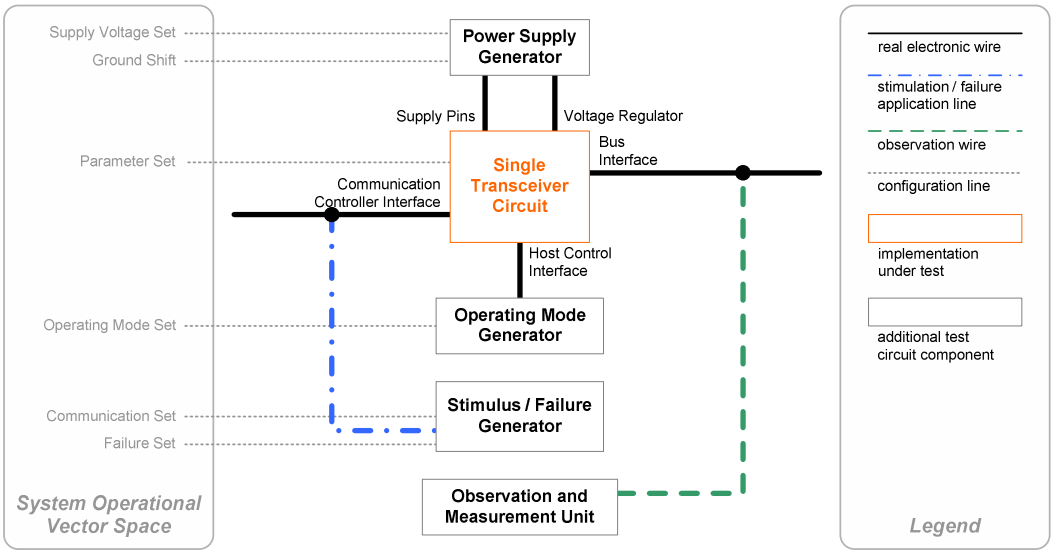
Description	This test shall ensure that the differential threshold voltage for indicating a dominant / recessive bus state between the bus pins *CANH* and *CANL* and the differential receiver hysteresis voltage is fulfilling the datasheet of the real device and follows the requirements of the transceiver model specification. The operating mode setup follows the device-dependent application notes for this test case by the semiconductor at model level 2 and 3. Matching Type: **Datasheet** Application Level: **1, 2, 3**
Setup	System Configuration: *single_trx* Parameter Set: *low_temp* | *typical* | *high_temp* Operating Mode: *normal* | *mode_semiconductor* Communication: *bus_ramp* Ground Shift: *static* Failure: *none*
Execution	The variation of the parameter set, operating mode and ground shift result into a sum of 9 test executions per implemented and applied operating mode and static ground shift. Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 2 nested parameter variations - at each execution, the analog and digital quantities are observed as described by the semiconductors application notes regarding this test case. - the minimum wake-up time via bus is measured according to the description of the semiconductors application notes regarding this test case. 
Response	The differential threshold voltage between the bus pins *CANH* and *CANL* and the computed differential receiver hysteresis voltage shall match exactly or lay within the limits of the given values in the corresponding datasheet of the transceiver device.
Reference	3.3, 3.4

4.1.4.2 Receiver Input Resistance

Description	This test shall ensure that the receiver input resistances at the bus pins are fulfilling the datasheet of the real device and follow the requirements of the transceiver model specification. Matching Type: **Datasheet** Application Level: **1, 2, 3**
Setup	System Configuration: *single_trx* Parameter Set: *low_temp* | *typical* | *high_temp* Operating Mode: *normal* | *low_power* Communication: *tx_const_high* Ground Shift: *none* Failure: *none*
Execution	The variation of the parameter set result into a sum of 3 test executions per operating mode. Conditions: - at model level 1, only the operating mode *normal* is applicable to this test case Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 1 nested parameter variations - at each execution, the input resistance is measured according to ISO11898 methods at the bus pins *CANH* and *CANL*. 
Response	The receiver input resistances at the bus pins *CANH* and *CANL* shall match exactly or lay within the limits of the given values in the corresponding datasheet of the transceiver device.
Reference	3.3

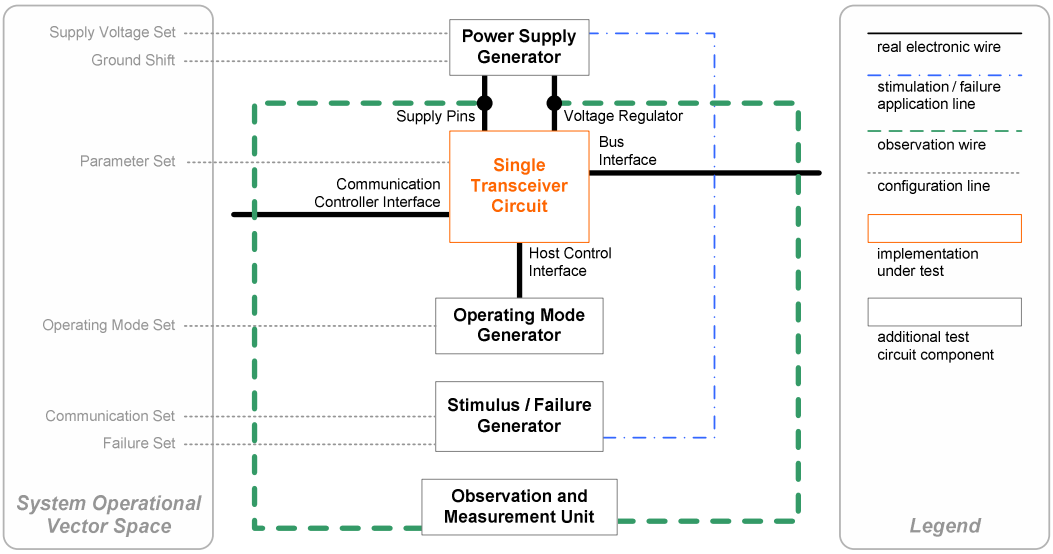
4.1.5 Common Mode Stabilization Output

4.1.5.1 Split Output Voltage

Description	This test shall ensure that the output voltage in loaded condition (see ISO11898-5]) at the *SPLIT* pin is fulfilling the datasheet of the real device and follows the requirements of the transceiver model specification. If no split pin is avaiable at the investigated device, this test case must not be executed. Matching Type: **Datasheet** Application Level: **1, 2, 3**
Setup	System Configuration: *single_trx* Parameter Set: *low_temp* | *typical* | *high_temp* Operating Mode: *normal* Communication: *split_cur_iso* Ground Shift: *none* Failure: *none*
Execution	The variation of the parameter set result into a total sum of 3 test executions. Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 1 nested parameter variations - at each execution, the output voltage is observed at the *SPLIT* pin of the transceiver according to ISO11898-5 (adjusted I_{SPLIT} within -500µA to 500µA) 
Response	The output voltage at the *SPLIT* pin shall match exactly or lay within the limits of the given values in the corresponding datasheet of the transceiver device.
Reference	3.3

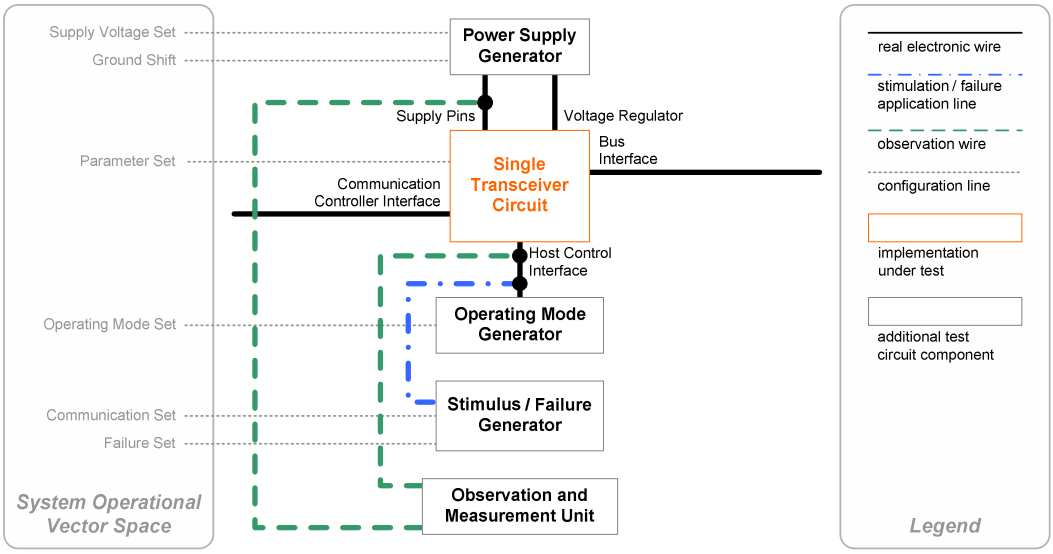
4.1.6 Inhibit Output

4.1.6.1 Inhibit High Level Voltage Drop

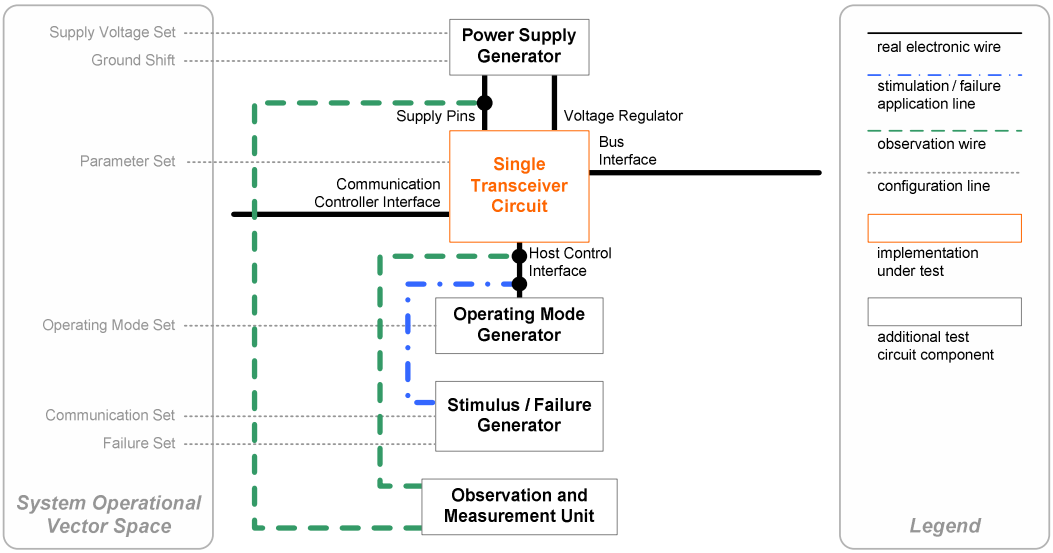
Description	This test shall ensure that the voltage drop at the *INH* pin is fulfilling the datasheet of the real device and follows the requirements of the transceiver model specification. Matching Type: **Datasheet** Application Level: **2, 3**
Setup	System Configuration: *single_trx* Parameter Set: *low_temp* | *typical* | *high_temp* Operating Mode: *normal* Communication: *inh_cur_ramp* Ground Shift: *none* Failure: *none*
Execution	The variation of the parameter set result into a total sum of 3 test executions. Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 1 nested parameter variations - at each execution, the output voltage is observed at the *INH* pin of the transceiver the difference between the battery supply voltage and the output voltage at *INH* marks the desired voltage drop value 
Response	The voltage drop at the *INH* pin shall match exactly or lay within the limits of the given values in the corresponding datasheet of the transceiver device.
Reference	3.3, 3.4

4.1.7 Wake Up

4.1.7.1 Wake Up Threshold Voltage

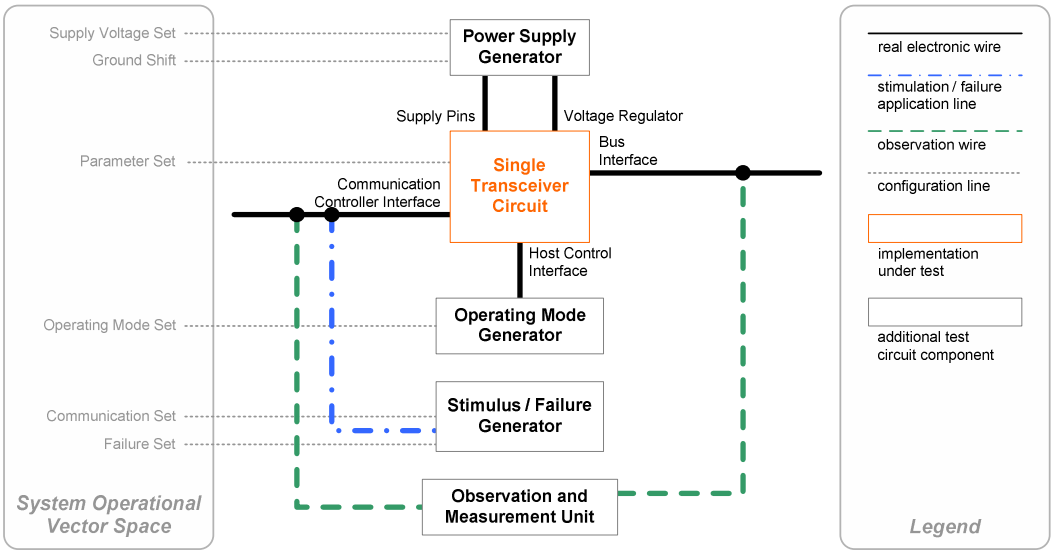
Description	This test shall ensure that the voltage threshold at the *WAKE* pin is fulfilling the datasheet of the real device and follows the requirements of the transceiver model specification. The operating mode setup follows the device-dependent application notes for this test case by the semiconductor. Matching Type: **Datasheet** Application Level: **2, 3**
Setup	System Configuration: *single_trx* Parameter Set: *low_temp* | *typical* | *high_temp* Operating Mode: *mode_semiconductor* Communication: *wake_ramp* Ground Shift: *none* Failure: *none*
Execution	The variation of the parameter set result into a device-dependent minimum power of 3 test executions. Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 2 nested parameter variations - at each execution, the voltage is observed at the *WAKE* pin and the power supply pins of the transceiver The wake-up threshold voltage marks the difference between the voltage at the power supply pin stated in the datasheet and the voltage at the *WAKE* pin 
Response	The wake-up threshold voltage between the datasheet-given power supply pin and the *WAKE* pin shall match exactly or lay within the limits of the given values in the corresponding datasheet of the transceiver device.
Reference	3.3, 3.4

4.1.7.2 Wake Up Input Current

Description	This test shall ensure that the input current at the *WAKE* pin at different logical levels is fulfilling the datasheet of the real device and follows the requirements of the transceiver model specification. Matching Type: **Datasheet** Application Level: **2, 3**
Setup	System Configuration: *single_trx* Parameter Set: *low_temp* | *typical* | *high_temp* Operating Mode: *normal* Communication: *wake_ramp* Ground Shift: *none* Failure: *none*
Execution	The variation of the parameter set result into a total sum of 6 test executions. Conditions: - for the voltages to apply at logical high or low level at *WAKE* pin, see the given values in the datasheet Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 2 nested parameter variations - at each execution, the input current is observed at the *WAKE* pin of the transceiver at the datasheet-given voltage levels for indicating logical high or logical low level at the *WAKE* pin 
Response	The input currents at the *WAKE* pin shall match exactly or lay within the limits of the given values in the corresponding datasheet of the transceiver device.
Reference	3.3, 3.4

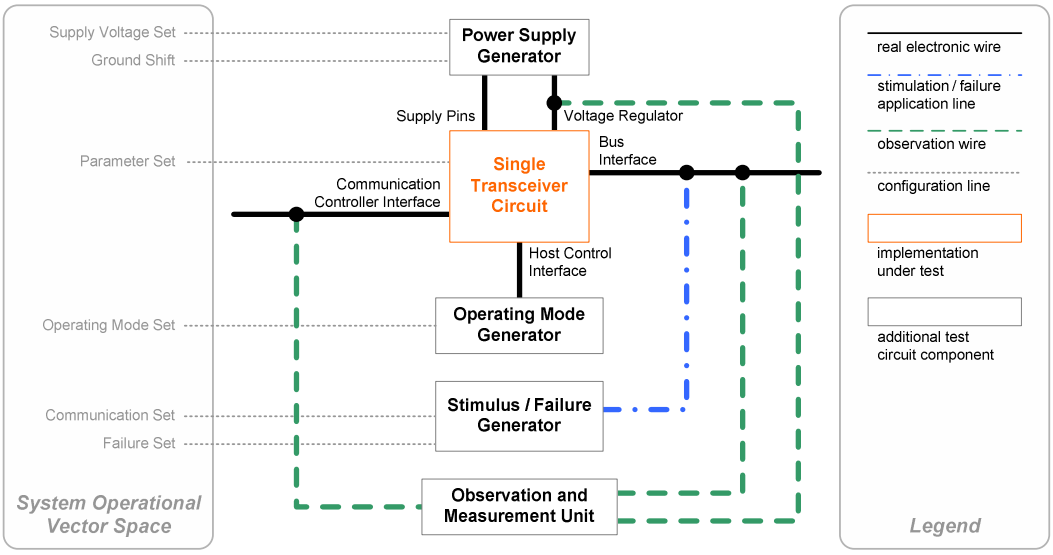
4.2 Dynamic Behaviour

4.2.1 Propagation Delays

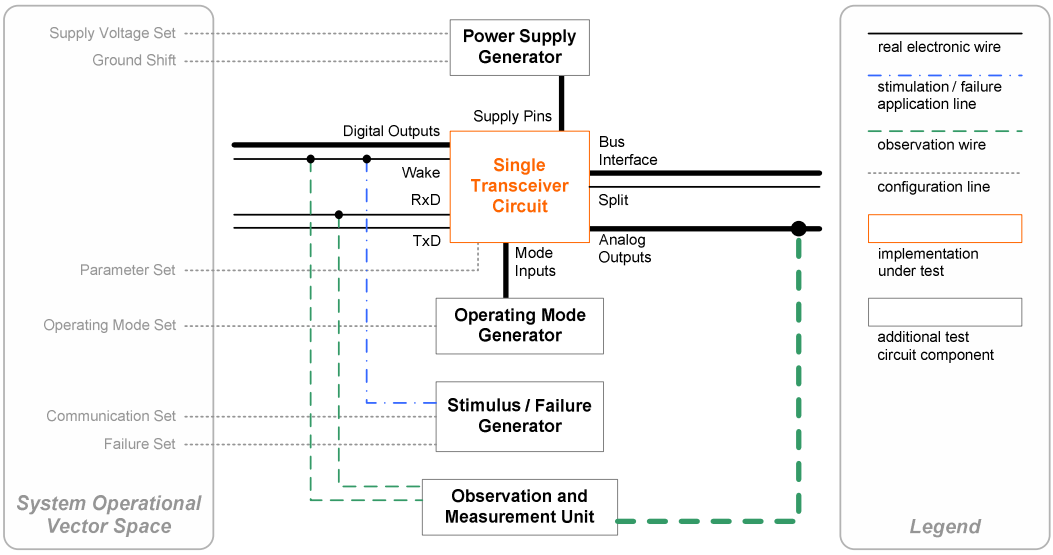
Description	This test shall ensure that the propagation delays between the *TxD*, Bus and *RxD* pins are fulfilling the datasheet of the real device and follows the requirements of the transceiver model specification. Matching Type: **Datasheet** Application Level: **1, 2, 3**
Setup	System Configuration: *single_trx* Parameter Set: *low_temp* | *typical* | *high_temp* Operating Mode: *normal* Communication: *tx_neg_pulse* Ground Shift: *none* Failure: *none*
Execution	The variation of the parameter set result into a total sum of 3 test executions. Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 1 nested parameter variations - at each execution, the in- and output levels are observed at the *TxD*, Bus and *RxD* pins of the transceiver - the delays are measured between the rising / falling edges between: *TxD* to Bus Bus to *RxD* *TxD* to *RxD* the thresholds for the logical levels are taken from the datasheet. 
Response	The propagation delays between *TxD*, Bus and *RxD* pins shall match exactly or lay within the limits of the given values in the corresponding datasheet of the transceiver device.
Reference	3.4

4.2.2 Wake Up

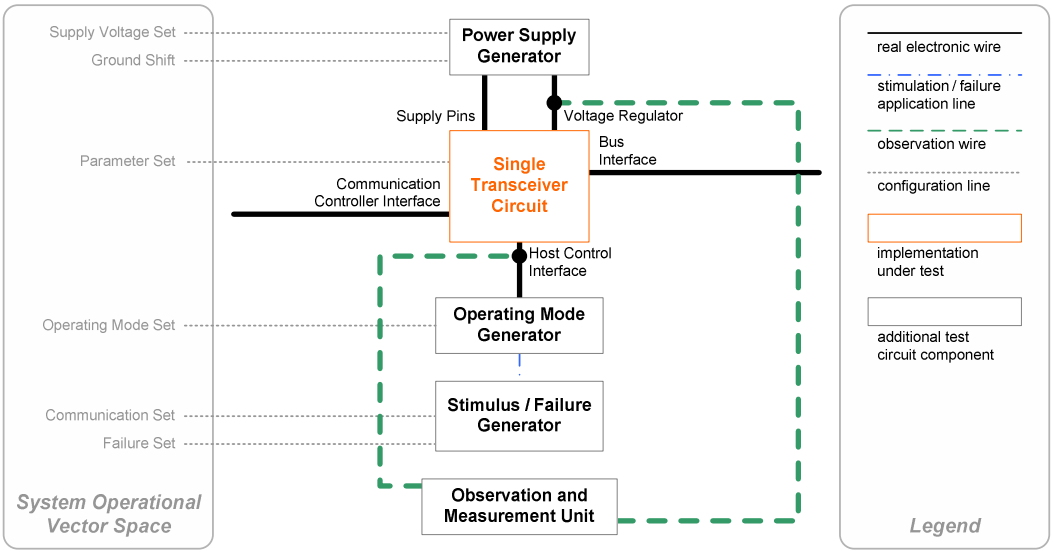
4.2.2.1 Wake Up via Bus

Description	This test shall ensure that the minimum wake up detection time via bus pins is fulfilling the datasheet of the real device and follows the requirements of the transceiver model specification. The operating mode and communication / stimulus setup follows the device-dependent application notes for this test case by the semiconductor. Matching Type: **Datasheet** Application Level: **2, 3**
Setup	System Configuration: *single_trx* Parameter Set: *low_temp* | *typical* | *high_temp* Operating Mode: *mode_semiconductor* Communication: *wbus_semiconductor* Ground Shift: *none* Failure: *none*
Execution	The variation of the parameter set result into a device-dependent minimum power of 3 test executions. Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 2 nested parameter variations - at each execution, the analog and digital quantities are observed as described by the semiconductors application notes regarding this test case. - the minimum wake-up time via bus is measured according to the description of the semiconductors application notes regarding this test case. The setup picture below shows schematically only an example for the device-dependent communication / stimulus setup. 
Response	The minimum wake-up detection time via bus shall match exactly or lay within the limits of the given values in the corresponding datasheet of the transceiver device.
Reference	3.4

4.2.2.2 Wake Up via Pin

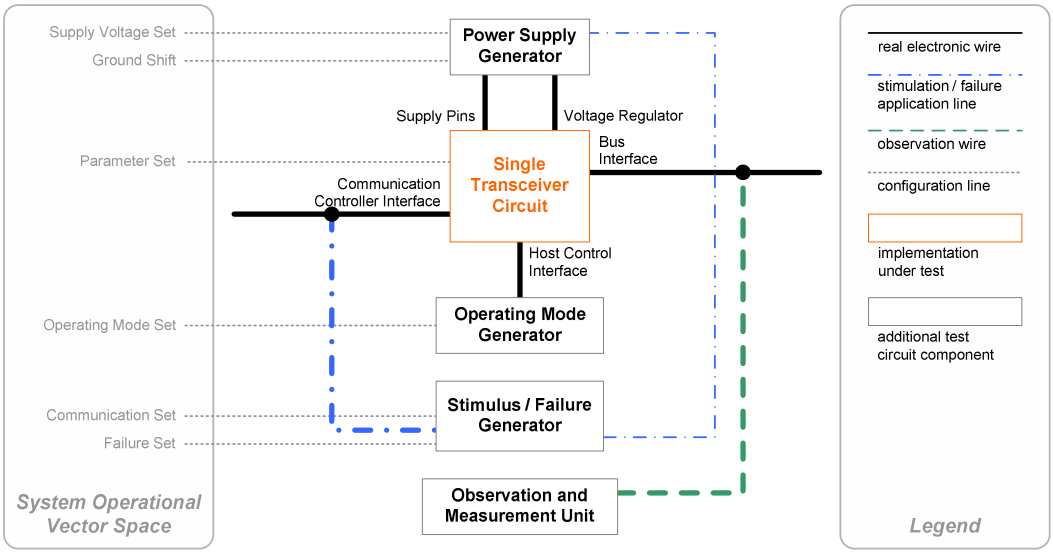
Description	This test shall ensure that the minimum wake up detection time via *WAKE* pin is fulfilling the datasheet of the real device and follows the requirements of the transceiver model specification. The operating mode and communication / stimulus setup follows the device-dependent application notes for this test case by the semiconductor. Matching Type: **Datasheet** Application Level: **2, 3**
Setup	System Configuration: *single_trx* Parameter Set: *low_temp* | *typical* | *high_temp* Operating Mode: *mode_semiconductor* Communication: *wpin_semiconductor* Ground Shift: *none* Failure: *none*
Execution	The variation of the parameter set result into a device-dependent minimum power of 3 test executions. Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 3 nested parameter variations - at each execution, the analog and digital quantities are observed as described by the semiconductors application notes regarding this test case. - the minimum wake-up time via bus is measured according to the description of the semiconductors application notes regarding this test case. The setup picture below shows schematically only an example for the device-dependent communication / stimulus setup. 
Response	The minimum wake-up detection time via *WAKE* pin shall match exactly or lay within the limits of the given values in the corresponding datasheet of the transceiver device.
Reference	3.4

4.2.3 Go to Sleep

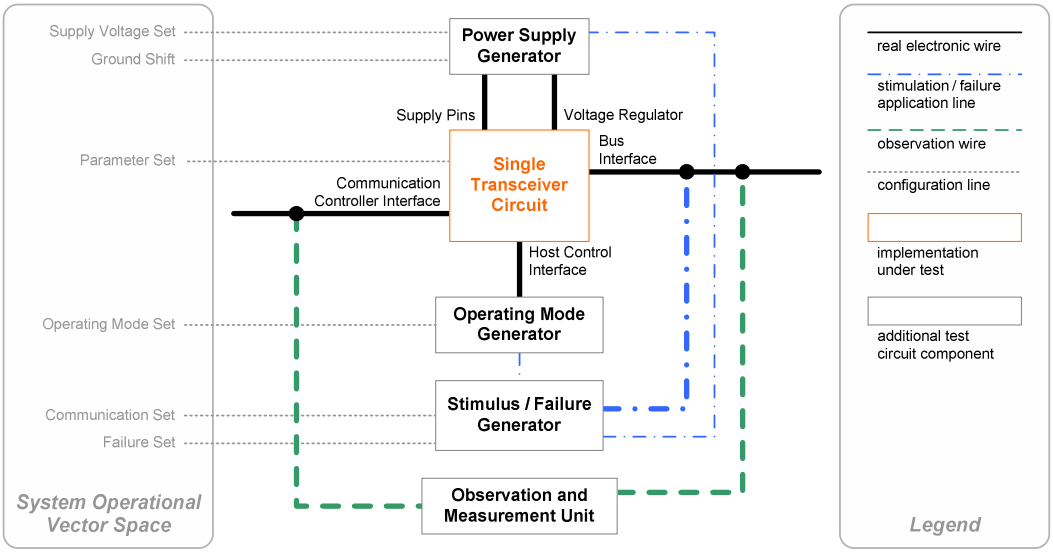
Description	This test shall ensure that the transceiver model switches into low power mode after the minimum hold time set of the go-to-sleep command at the mode control input pins with the prescribed values in the datasheet of the real device and follows the requirements of the transceiver model specification. Matching Type: **Datasheet** Application Level: **2, 3**
Setup	System Configuration: *single_trx* Parameter Set: *low_temp* | *typical* | *high_temp* Operating Mode: *normal* | *low_power* | *mode_semiconductor* Communication: *goto_sleep* Ground Shift: *none* Failure: *none*
Execution	The variation of the parameter set and operating mode result into a sum of 3 test executions per operating mode. Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 2 nested parameter variations - at each execution, the voltage is observed at the *INH* pin of the transceiver - the time difference between the go-to-sleep command via *OPM0* and *OPM1* pins and the deactivation transition at the *INH* pin (pulled down to ground) marks the minimum hold time for go-to-sleep. The thresholds for the logical levels are taken from the datasheet. 
Response	The minimum hold time for go to sleep command shall match exactly or lay within the limits of the given values in the corresponding datasheet of the transceiver device.
Reference	3.4

4.2.4 Signal Integrity

4.2.4.1 Signal Shape

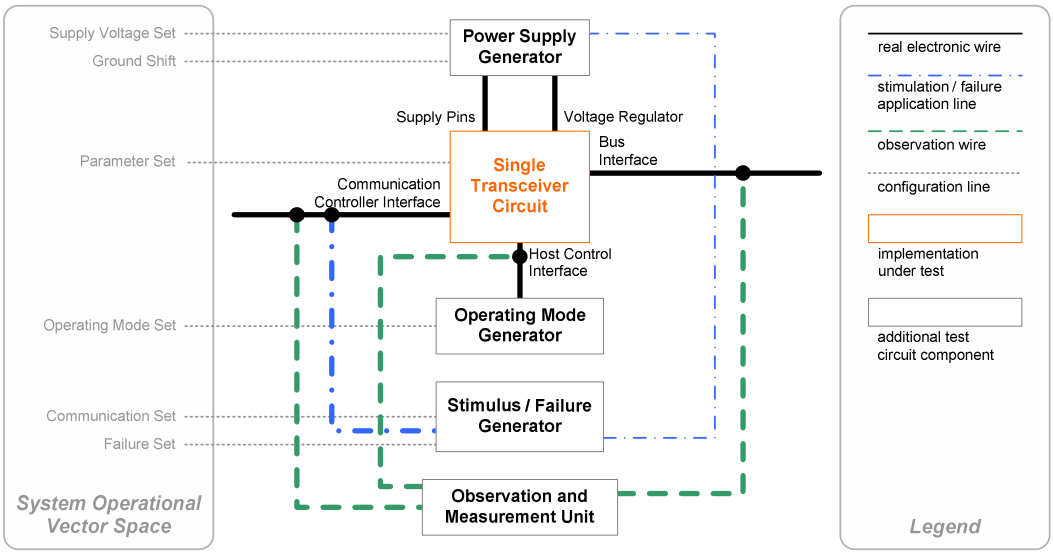
Description	This test checks the signal shape of the transmitter output stage, with its rise and fall times between bus state transitions and that these can be compared with real measurements to verify a correct mapping from the real device to the model. Matching Type: **Real Device Measurement** Application Level: **1, 2, 3**
Setup	System Configuration: *single_trx* Parameter Set: *typical* Operating Mode: *normal* Communication: *tx_neg_pulse* Ground Shift: *static* | *dynamic* Failure: *none*
Execution	The variation of the ground shift result into a total sum of 4 (3 different static values) executions. Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 1 nested parameter variations - at each execution, the voltage is observed between the bus pins *CANH* / *CANL* of the transceiver - the rise and fall times of the bus state transitions are measured with the logical level thresholds taken from the datasheet 
Response	The rise and fall times at the bus pins *CANH* / *CANL* compared with real measurements shall converge.
Reference	3.4

4.2.4.2 Receiver max. Common Mode Offset

Description	This test checks at which offset at the common mode operation, due to ground shift variations, the receiver recognizes the right data applied at the bus. It also checks if the observed behaviour corresponds to the behaviour in a real device measurement. Matching Type: **Real Device Measurement** Application Level: **1, 2, 3**
Setup	System Configuration: *single_trx* Parameter Set: *typical* Operating Mode: *normal* Communication: *bus_dom_pulse* Ground Shift: *static* | *dynamic* Failure: *none*
Execution	The variation of the ground shift result into a total sum of 4 (3 different static values) test executions. Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 1 nested parameter variations - at each execution, the in- and output levels are observed at the *RxD* pin and at the bus pins *CANH* / *CANL* of the transceiver - the rise and fall times of the bus and *RxD* state transitions are measured with the logical level thresholds taken from the datasheet - the logical level between the *RxD* pin and the logical level taken by the difference between *CANH* / *CANL* pins is compared 
Response	The compared logical levels and the voltages between the *RxD* and *CANH* / *CANL* pins shall converge with real device measurements.
Reference	3.4

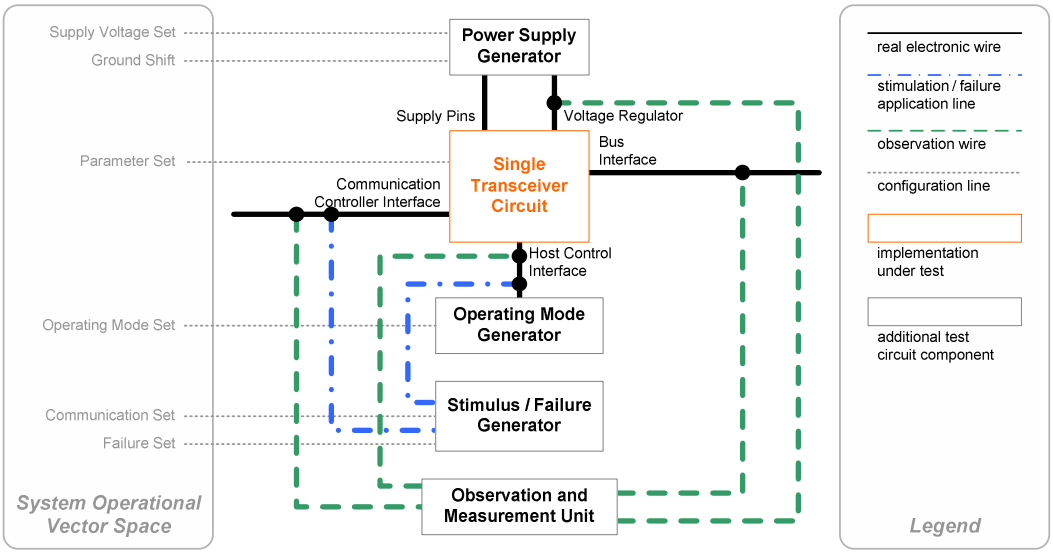
4.2.5 Signal Integrity (Multi Node Environment)

4.2.5.1 Signal Shape within Star Topology

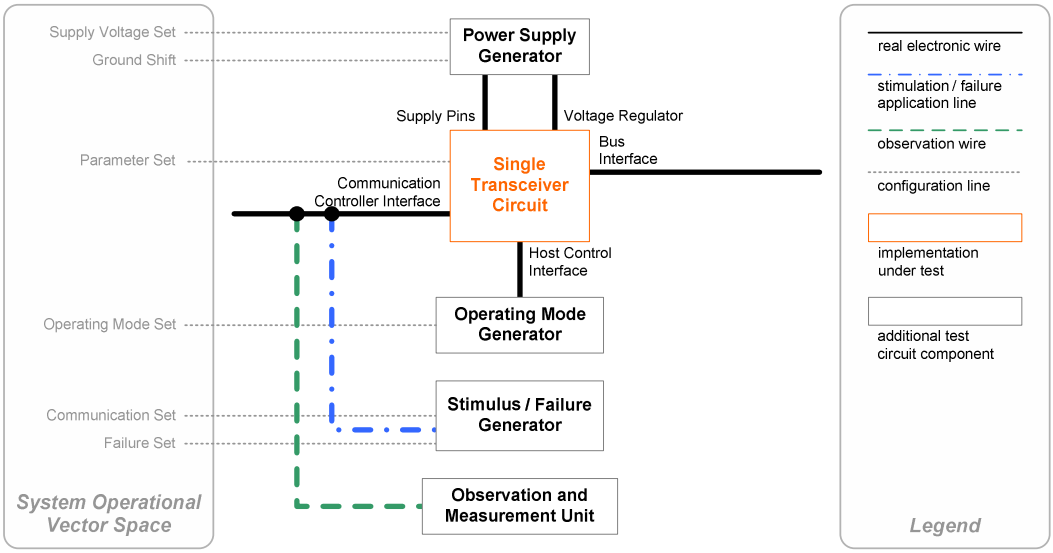
Description	This test checks the signal shape of the transceiver in a multinode environment with ground shift variations, the receiver recognizes the right data applied at the bus. It also checks if the observed behaviour corresponds to the behaviour in a real device measurement. Matching Type: **Real Device Measurement** Application Level: **1, 2, 3**
Setup	System Configuration: *star_topology* Parameter Set: *typical* Operating Mode: *normal* Communication: *tx_round_robin* Ground Shift: *static* | *dynamic* Failure: *none*
Execution	The variation of the ground shift result into a total sum of 4 (3 different static values) test executions with all 8 nodes being stimulated. Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 1 nested parameter variations - at each execution, the voltage is observed at the *RxD* and *SPLIT* pins and at the bus pins *CANH* / *CANL* of all transceivers in the topology - the logical level between the *RxD* pin and the difference between *CANH* / *CANL* pins is compared from each transceiver The setup picture below shows schematically only one node of the given topology. The test circuit from the setup picture is applied to all nodes in the topology. 
Response	The measured signal shapes at the bus pins *CANH* / *CANL* at each transceiver in the topology shall converge with the signal shapes of the real measurement.
Reference	3.4

4.2.6 Network State Transitions (Multi Node Environment)

4.2.6.1 Sequential Wake Up

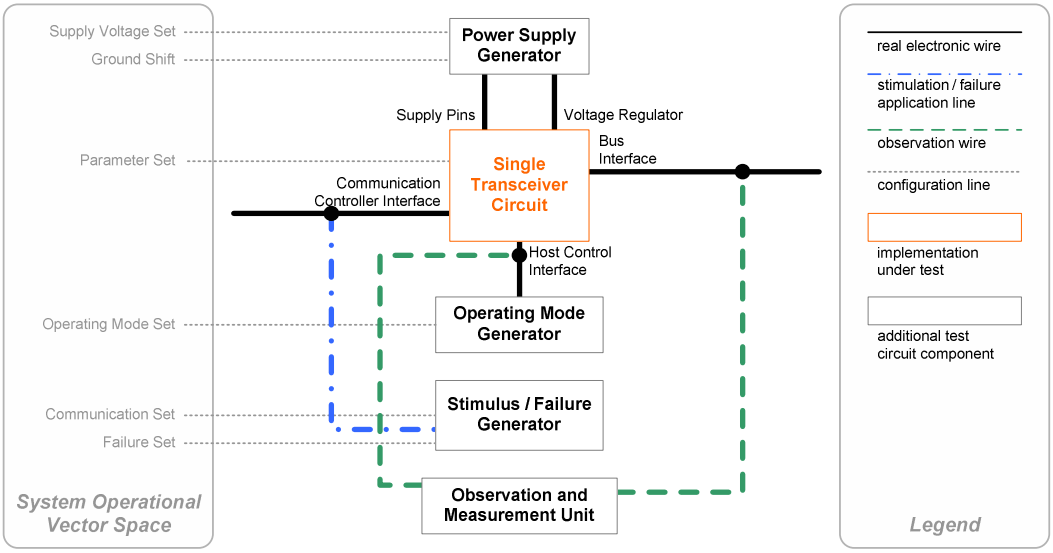
Description	This test shall ensure proper operation of all of the transceivers in the topology according to the datasheet requirements of the transceiver and transceiver model specification. In this case, one node gets waked up via *WAKE* pin and sends a dominant bit to the bus to wake up the others nodes via bus. Matching Type: **Datasheet** Application Level: **2, 3**
Setup	System Configuration: *star_topology* Parameter Set: *low_temp* | *typical* | *high_temp* Operating Mode: *low_power* | *mode_semiconductor* Communication: *tx_two_nodes* Ground Shift: *none* Failure: *none*
Execution	The variation of the parameter set result into a sum of 3 test executions per operating mode with 2 nodes being stimulated. Conditions: - the *tx_two_nodes* communication starts after node 8 had been woken up via pin, the others are waked up via the sent dominant bit at the bus of the already woken up transceiver. - at this test case, the implemented *mode_semiconductor* operating modes shall be equivalent to (additional) low power modes. Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 1 nested parameter variations - at each execution, the in- and output levels are observed at the *INH* and *RxD* pins of all transceivers in the topology and the bus lines *CANH* / *CANL* The setup picture below shows schematically only one node of the given topology. The test circuit from the setup picture is applied to all nodes in the topology, except the stimulus application. 
Response	The voltages and logical levels at all *INH* and *RxD* pins shall indicate correct functionality according to the transceiver specification. That means every transceiver shall receive all of the sent dominant bits and the first dominant bit being used to wake up, except the transceiver being woke up via *WAKE* pin.
Reference	3.4

4.2.7 Ringing Behaviour (Multi Node Environment)

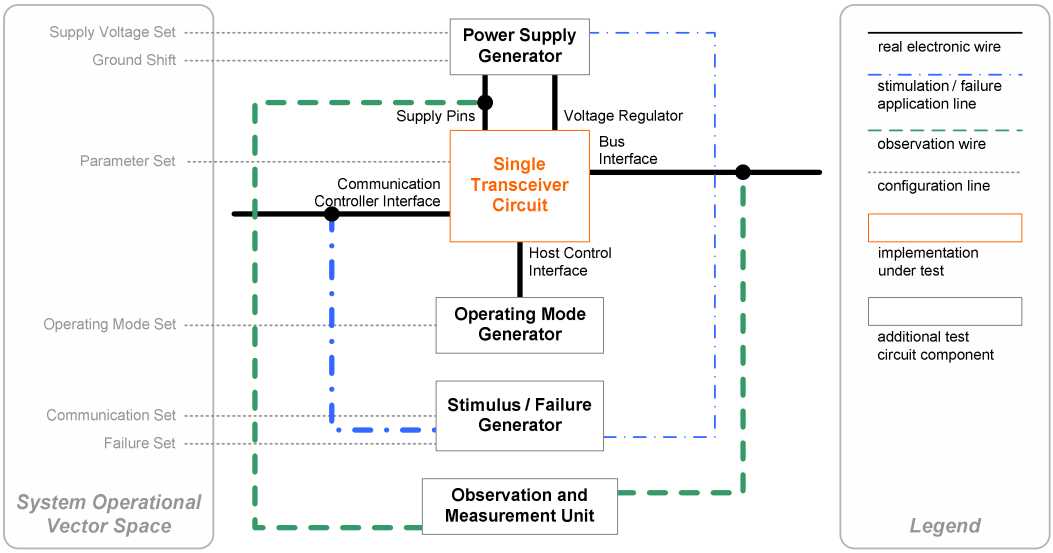
Description	This test shall ensure that the ringing behaviour of the transceiver within a topology can be observed and compared against real device / topology measurements. Matching Type: **Real Device Measurement** Application Level: **1, 2, 3**
Setup	System Configuration: *star_topology* Parameter Set: *typical* Operating Mode: *normal* Communication: *tx_round_robin* Ground Shift: *none* Failure: *none*
Execution	No variation of the setup results into 1 test execution with all 8 nodes being stimulated. Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 1 nested parameter variations - at each execution, the output level is observed at the *RxD* pin of all the transceivers in the topology. The setup picture below shows schematically only one node of the given topology. The test circuit from the setup picture is applied to all nodes in the topology. 
Response	An informational result shall be included in the documentation.
Reference	3.4

4.3 Error Behaviour

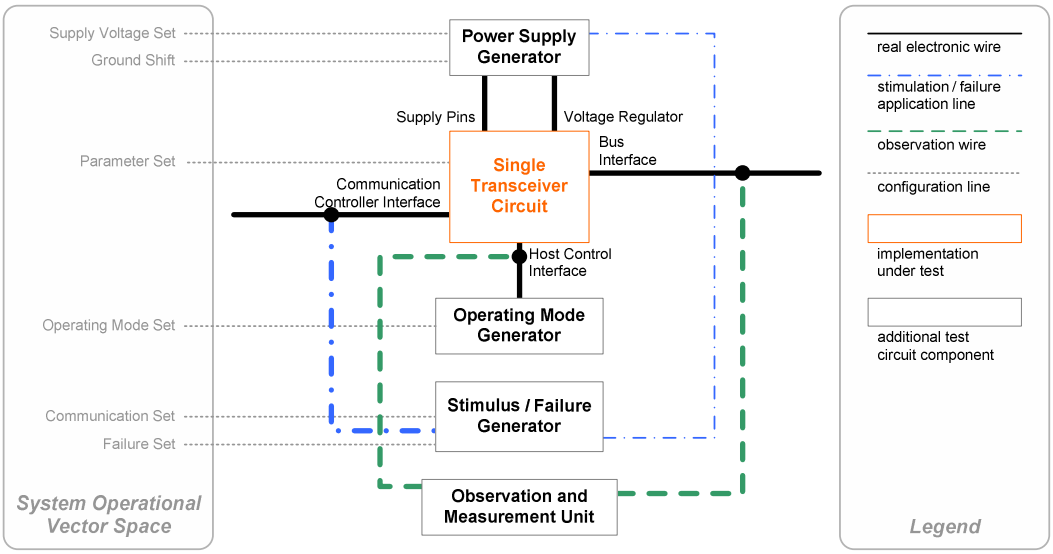
4.3.1 TXD Dominant Time-Out

Description	This test shall ensure that the *TxD* dominant time-out diagnosis value is fulfilling the datasheet of the real device and follows the requirements of the transceiver model specification. In this case, the *TxD* pin is stimulated with a very long timed dominant state to indicate the erroneous behaviour. Matching Type: **Datasheet** Application Level: **3**
Setup	System Configuration: *single_trx* Parameter Set: *low_temp* | *typical* | *high_temp* Operating Mode: *normal* Communication: *tx_falling_edge* Ground Shift: *none* Failure: *none*
Execution	The variation of the parameter set result into a total sum of 3 test executions. Conditions: - after the falling edge, the low voltage level at *TxD* is held for minimum 1000*t_{Bit} Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 1 nested parameter variations - at each execution, the voltage is observed at the bus pins *CANH* / *CANL* of the transceiver - the measured time difference between the falling edge at *TxD* and the bus state change into a non-dominant state marks the *TxD* dominant time-out value. If diagnostic output pins are implemented, they shall be observed, too. 
Response	The *TxD* dominant time-out value of shall match exactly or lay within the limits of the given values in the corresponding datasheet of the transceiver device. The bus state shall change to non-dominant state after the time-out. If diagnostic outputs are implemented, these have to reflect the states described in the datasheet for this type of error.
Reference	3.4

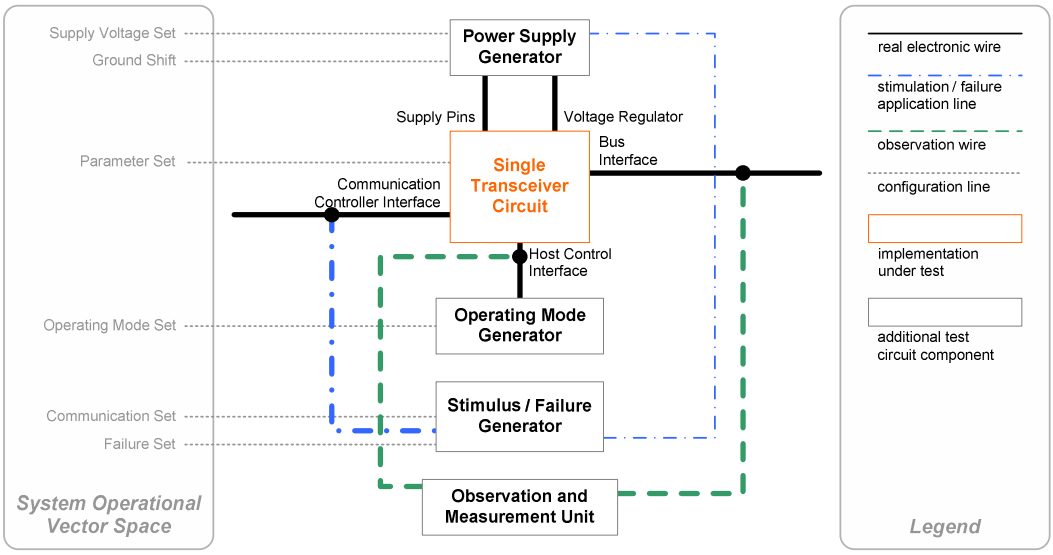
4.3.2 Undervoltage Detection Filter Time

Description	This test shall ensure that the filter time for the undervoltage detection at the power supply input pin(s) is fulfilling the datasheet of the real device and follows the requirements of the transceiver model specification. In this case, the supply voltages are set to the voltage level of the *GND* pin of the transceiver to indicate the undervoltage drop as a kind of loss of power failure. Matching Type: **Datasheet** Application Level: **2, 3**
Setup	System Configuration: *single_trx* Parameter Set: *low_temp* | *typical* | *high_temp* Operating Mode: *normal* Communication: *tx_const_high* Ground Shift: *none* Failure: *loss_power*
Execution	The variation of the parameter set and operating mode result into a sum of 3 test executions for each power supply pin. Conditions: - the *loss_power* error is applied at each power supply pin at a time. Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 2 nested parameter variations - at each execution, the voltages are observed at the power supply pin (where the voltage drop gets applied per loss of power failure application) and at bus pins *CANH* / *CANL* of the transceiver. When the transceiver switches internally into low power mode after the undervoltage detection, the bus state should change to high-ohmic / floating. The difference between the supply voltage drop and the change of the bus state marks the undervoltage detection filter time. 
Response	The measured undervoltage detection filter time shall match exactly or lay within the limits of the given values in the corresponding datasheet of the transceiver device.
Reference	3.4

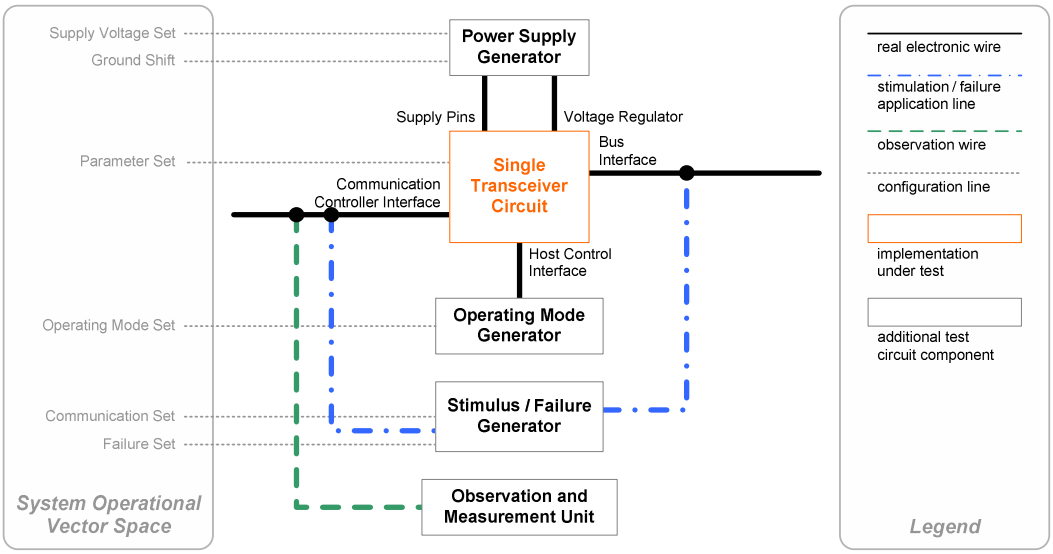
4.3.3 Loss of Power (Multi Node Environment)

Description	This test shall ensure the correct functional behaviour when power supply of a transceiver gets lost versus real device measurement. In this special case the supply voltages are set to ground connection. Matching Type: **Real Device Measurement** Application Level: **1, 2, 3**
Setup	System Configuration: *star_topology* Parameter Set: *typical* Operating Mode: *normal* Communication: *tx_two_nodes* Ground Shift: *none* Failure: *loss_ power*
Execution	No variation of the setup result into 1 test execution with 2 nodes being stimulated. Conditions: - only node 8 gets all of its power supplies lost Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 1 nested parameter variations - at each execution, the power supplies are set to the voltage level of the *GND* pin. The voltage is observed at the *SPLIT* pin and bus lines *CANH* / *CANL*. The input impedance at the bus pins *CANH* / *CANL* at the node with lost power being measured according to ISO11898 methods for measuring impedances. The setup picture below shows schematically only one node of the given topology. The test circuit from the setup picture is applied to all nodes in the topology, except the stimulus and failure application. 
Response	The input impedance and signal levels at the *SPLIT* pin and bus lines *CANH* / *CANL* shall reflect the behaviour of the real device. If diagnostic outputs are implemented (level 3 model implementation), these have to reflect the states described in the datasheet for this type of error.
Reference	3.4

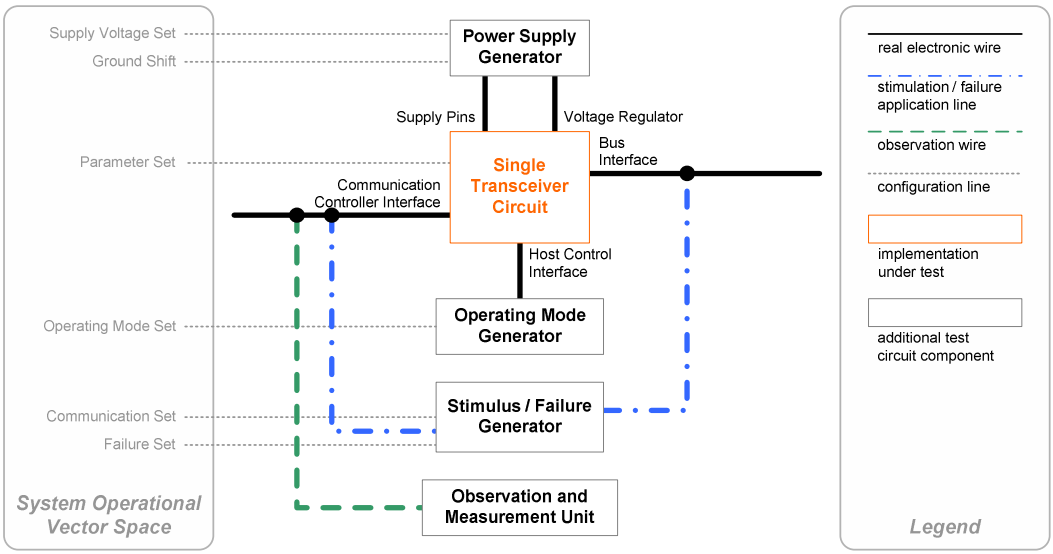
4.3.4 Loss of Ground (Multi Node Environment)

Description	This test shall ensure the correct functional behaviour of the transceiver if its ground connection gets lost versus real device measurement. In this special case, the ground connection is set to the supply voltage set value. Matching Type: **Real Device Measurement** Application Level: **1, 2, 3**
Setup	System Configuration: *star_topology* Parameter Set: *typical* Operating Mode: *normal* Communication: *tx_two_nodes* Ground Shift: *none* Failure: *loss_ground*
Execution	No variation of the setup result into 1 test execution with 2 nodes being stimulated. Conditions: - Only at node 8 the loss of ground error is getting applied Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 1 nested parameter variations - at each execution, the voltages at *GND* pin and all power supply pins except the battery supply pin are set to the battery supply voltage level of the V_{BAT} pin. the voltage is observed at the *SPLIT* pin and the bus lines *CANH* / *CANL*. The impedance of the bus lines *CANH* / *CANL* being measured according to ISO11898 methods for measuring impedances. The setup picture below shows schematically only one node of the given topology. The test circuit from the setup picture is applied to all nodes in the topology, except the stimulus and failure application. 
Response	The input impedance and signal levels at the *SPLIT* pin and the bus lines *CANH* / *CANL* shall reflect the behaviour of the real device. If diagnostic outputs are implemented (level 3 model implementation), these have to reflect the states described in the datasheet for this type of error.
Reference	3.4

4.3.5 Short Circuit (Multi Node Environment)

Description	This test shall ensure the correct functional behaviour of the transceivers in the topology when short circuit condition arises at the bus lines. In this case, one transmission line wire is shortened at a time at either ground, power supply or the other transmission line wire in the topology and the communication between the nodes is getting checked. Matching Type: **Real Device Measurement** Application Level: **1, 2, 3**
Setup	System Configuration: *star_topology* Parameter Set: *typical* Operating Mode: *normal* Communication: *tx_two_nodes* Ground Shift: *none* Failure: *canh_to_canl* | *canh_to_gnd* | *canh_to_pwr* | *canl_to_gnd* | *canl_to_pwr*
Execution	The variation of the parameter set and failure result into a total sum of 5 test executions with 2 nodes being stimulated. Conditions: - Only at node 8 the short circuit error is getting applied Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 1 nested parameter variations - at each execution, the output level is observed at the *RxD* at all transceivers in the topology The setup picture below shows schematically only one node of the given topology. The test circuit from the setup picture is applied to all nodes in the topology, except the stimulus and failure application. 
Response	The signal level at the *RxD* pins shall reflect the behaviour of the real device. If diagnostic outputs are implemented (level 3 model implementation), these have to reflect the states described in the data-sheet for this type of error.
Reference	3.4

4.3.6 Open Wire (Multi Node Environment)

Description	This test shall ensure the correct functional behaviour of the transceivers in the topology when one of the bus lines is opened. In this case, a wire at one node in the topology is opened and the communication between the nodes is getting checked. Matching Type: **Real Device Measurement** Application Level: **1, 2, 3**
Setup	System Configuration: *star_topology* Parameter Set: *typical* Operating Mode: *normal* Communication: *tx_two_nodes* Ground Shift: *none* Failure: *canh_open* | *canl_open*
Execution	The variation of the parameter set and failure result into a total sum of 2 test executions with 2 nodes being stimulated. Conditions: - Only at node 8 the open wire error is getting applied Steps: - the system is set to the initial state specified by the setup above - the setup variations are executed in 2 nested parameter variations - at each execution, the output level is observed at the *RxD* pin at all transceivers in the topology The setup picture below shows schematically only one node of the given topology. The test circuit from the setup picture is applied to all nodes in the topology, except the stimulus and failure application. 
Response	The signal level at the *RxD* pin shall reflect the behaviour of the real device. If diagnostic outputs are implemented (level 3 model implementation), these have to reflect the states described in the data-sheet for this type of error.
Reference	3.4

5 Appendix

5.1 Generic Constants

Generic Name	Generic Value
t_{Bit}	2 µs
t_{rise}	15 ns
t_{fall}	15 ns
r_star_term	60 Ω
r_openwire	1 tΩ
t_{Ramp}	1000 * t_{UVdet}
t_{UVdet}	see datasheet for undervoltage detection filter time
I_0	0 µA
I_{INH}	see datasheet of the transceiver

5.2 References

[1] **Controller area network,**
- *Data link layer and physical signalling*
  International Standard, ISO 11898-1, 2003-12
- *High-speed medium access unit*
  International Standard, ISO 11898-2, 2003-11
- *High-speed medium access unit with low-power mode*
  International Standard, ISO 11898-5, 2007-06

[2] **Requirement Specification for Transceiver Simulation Models,**
Transceiver Model Specification V1.1
GIFT/ICT, 2010-02

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