CAN FD Network Validation

Simulation, validation criteria and an automated evaluation

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ABSTRACT: The CAN protocol with flexible data rate (CAN FD) addresses the increasing demands on automotive system bandwidth offering an easier adaptability and high re-use factor of CAN, the most disseminated in-vehicle network protocol. However, it brings new challenges to the designers. Since the dynamic behavior of the system cannot be predicted by manual calculations, the developers are required to use the simulation to analyze the network design for a robust layout and to investigate the influences of new components with two main goals: improving the signal quality and ensuring a correct communication with precise results even under worst case environmental conditions. Simulation is the only way to determine the asymmetry of each bit caused by physical layer effects and to analyze the behavior of the digital and analogue signal. In order to obtain a design of robust CAN FD networks, developers are faced with a lot of variations causing a significant amount of data to be analyzed and therefore automatization and the usage of precise simulators and models are decisive factors to address it properly.

KEY WORDS: simulation, model development, VHDL-AMS, automation, validation criteria, CAN FD evaluation, arbitration phase, data phase, signal symmetry, analogue ringing, verification, laboratory measurement

1. INTRODUCTION

This paper shows how to define and develop a robust design methodology based on a virtual prototype implementation of a CAN FD network, which criteria should be considered and how the entire design flow and evaluation can be automated to get an efficient simulation process, while decreasing the analysis periods and costs. CAN FD is a further building block, helping to close the gap between the growing needs regarding the exchange of information from electronic units and the currently available technologies. The protocol is indeed based on the well-known CAN 2.0b technology but additional criteria need to be considered for the topology validation. This document also depicts an automated design flow, which is based on simulation, measurements and verification of a topology design. Its current main focus is the CAN FD technology, which is a new version of the classical CAN protocol and allows transmitting larger payloads even at higher frequency. Nevertheless, the whole process is also applicable for CAN, FlexRay and LIN. The main objective of this document is to describe the importance that simulation is acquiring nowadays due to a constant increase of quality and performance requirements within in-vehicle networks (IVN). Physical layer analysis is the key to obtain a robust design. One question coming from a designer may be: "Why should I simulate?", which results in the following simulation advantages:

- Quality assurance
- Broader analysis compared to laboratory measurements or vehicle level test(s)
- Total cost reduction
- Short development time

Without the help of simulation, a measurement will only disclose a single outcome, generally the most likely or average scenario. In reality it is not possible to reproduce the worst case condition because the values of the different parameters of each component are fixed somewhere in the probability distribution curve. The question in fact is: Does one measurement of a prototype network represent the measurement for all production? Due to the fact that simulation can cover all possible worst case scenarios, only with simulation, the answer will be positive. Simulation is therefore the most important phase during the validation process of a modern topology.

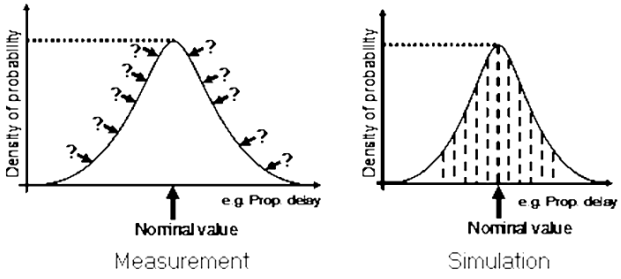

Fig. 1 Difference between simulation and measurement

The simulation of IVN is based on VHDL-AMS models. VHDL-AMS is a hardware description language used for the description and the simulation of analog, digital and mixed-signal systems. VHDL itself is an acronym of 'Very High Speed Integrated Circuit Hardware Description Language' and AMS, 'Analog and Mixed-Signal' as extension. VHDL is defined in IEEE Std. 1076-1993, and VHDL-AMS is a strict superset of it. Thus any model valid in VHDL 1076 is valid in VHDL-AMS and yields the same simulation results. There are many advantages to using VHDL-AMS for modeling and simulation. It supports multiple modeling domains so its coverage of represented systems is wide: electrical, mechatronic, hydraulic, and so on. Additional to that, these multi domain models can be intermixed in a design and simulated together. Mixed signal support enables design and verification of digital control logic simultaneously with analog system behavior. An implicit solver has the flexibility to control accuracy and simulation speed. VHDL-AMS is a standardized language so models written in it have high a level portability, which enables model exchange between groups, divisions, and companies through a model supply chain. In addition to IVN validation, the system simulation model can be leveraged in various applications related to automotive electrification. For example, a powertrain using inverter, motor, regenerative braking, and chemical battery, power control unit using power semiconductor and thermal cooling, wire harness for power and signal transmission and so on. Simulation can be done in a wide range of abstraction including the import of FEM results to system dynamics models.

2. IVN VALIDATION VIA SIMULATION

The first and most important phase in validating a modern topology design is the simulation phase. The trend shows an ever increasing evaluation of vehicle networks using simulation. With the need of simulations of CAN FD networks, this trend will be further intensified. The main goal of the simulation is to achieve a confidence level on the designed topology. Once the design is approved, it can be implemented in either a laboratory or vehicle. Simulation involves accurate models for transceivers and cables as well as a simulation environment, controllable by means of scripting, thus automatization. A previous requirement to the topology simulation is the model development. After having a plausible model, the topology verification can be executed.

2.1. Model development

The development of a model is an important step in the design verification flow. The simulation is compared with laboratory measurements and it must reflect the curve shaping of the real device. The tests are executed for a device with its typical load conditions. On the other side, when the model shows the same behavior as the real device, a test within a network must be executed, consisting once more in the comparison between the simulation and the real measurements.

2.2. Implementation and methodology

The main goal from the designer's point of view is to achieve a quality assurance of its own design. The robustness of the system is evaluated within the simulation process and the final results should be compared with some specific laboratory measurements for verification. Particularly in CAN FD networks, the usage of simulation is mandatory since the asymmetry of the signal edges plays a very important role. Marginal environmental conditions, such as high or low temperatures, can additionally intensify negative effects on the asymmetry of the signal edges, which can be analyzed easily by simulation. Since CAN FD is based on the classical CAN, the arbitration is to be considered equal. The same rules and limits for the arbitration phase, as in the CAN protocol, are still valid. In this document such rules are not contemplated. However, new additional rules should be considered for the data phase in order to judge the mentioned asymmetry of the signal edges. The asymmetries of the measured edges within a network essentially determine the choice of the actual sampling point position during the data phase.

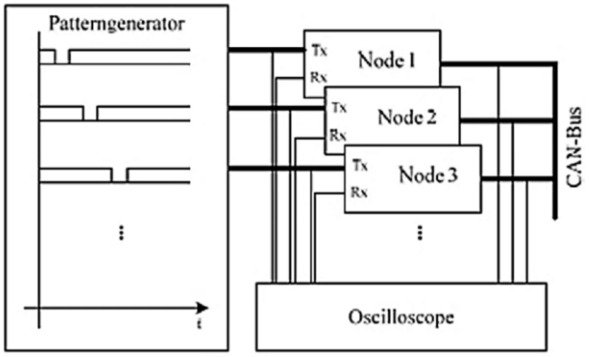

Fig. 2 Simulation setup

A round robin communication will be initiated at the simulation of the topology. Each node acts once as a transmitter one after the other and sends a simple pattern to the bus. A pattern generator creates a digital input signal to the TxD pin of the transceiver with the required data rate, over the entire system. The resulting signals at the digital and analogous side were logged for a subsequent signal processing. With all of the collected signals, it is possible to calculate the propagation delays as well as the differential bus signals. The quality of the signal is analyzed at each node within the topology.

2.2.1. Stimulus signal

The stimulus pattern for each active transmitting ECU is a simple combination of consecutive bits. Depending on the test case, the bit stream contains one or several logical high bit (recessive), followed by one or several logical low (dominant) bit. A typical scenario is used when 5 dominant bits are followed by an unique recessive bit, then again a few more bits with dominant state. The combination of five consecutive dominant bits and a recessive bit assures the worst condition after charging the capacitances in the network for a total time equivalent to the five consecutive dominant bits and then discharge the capacitances only during one bit wide. If there is ringing in the network, this condition should expose it at its worst condition. In this way, the recessive bit (t_{REC}) is in between two dominant bits and the receiver must be able to detect this recessive bit.

2.2.2. Validation criteria

The most important criterion for a correct and robust CAN FD communication are the consideration of the clock tolerance, which depends on the bit timing and the safe sampling of each bit. While the requirements for the clock tolerance concentrate on the bit timing only and do not involve topology effects, the safe sampling of each bit is focused on the different propagation delays for a dominant to recessive edge and vice versa. The higher the baud rate is the more important the symmetry between the propagation delays of both edges becomes. This leads to an especial analysis regarding the timing components a transmission from one node to another requires. The following are parts of a detailed timing analysis in Figure 3:

$t_{CC\,T}$	Delay of the communication controller for internally activating the transmitted bit until it is available on the output pin
$t_{TRX\,T}$	Transmitter delay of the transceiver from changing the input signal until a first recognition on the output pin
t_{EMC}	Negative effects like EMC jitter
t_{WIRE}	Wiring propagation delay
$t_{TRX\,R}$	Receiver delay of the transceiver from crossing the threshold voltage until changing the state on the output pin
$t_{CC\,R}$	Delay of the communication controller from changing the input signal until internally recognition of the bit
$_{DR}$	Dominant-to-recessive edge
$_{RD}$	Recessive-to-dominant edge
t_{DBT}	Bit time of the data phase

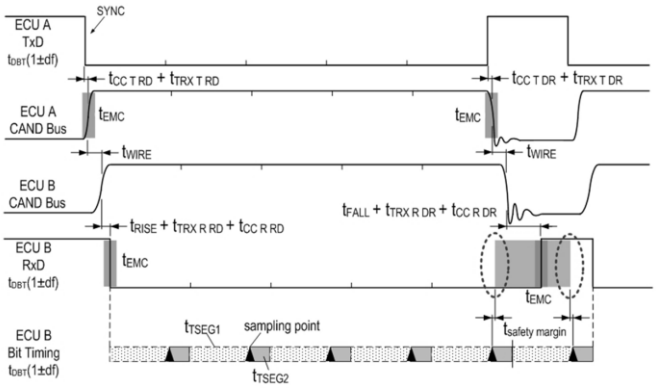

Fig. 3 Propagation delays and asymmetrc effects during a communication between two different nodes

To guarantee the stability of CAN FD, an additional safety margin before and after the sampling point needs to be defined. The measured recessive bit time t_{REC} is taken as the nominal bit time minus all the following parameters in the signal:

$$t_{REC} = t_{DBT} - (t_{TRX\,T\,DR} - t_{TRX\,T\,RD}) - (t_{TRX\,R\,DR} - t_{TRX\,R\,RD}) - (t_{FALL} - t_{RISE})$$

With these definitions, the following inequalities are to be contemplated for the worst case condition:

- Supposing that ECU A is faster than ECU B, at the 5th bit of the observed RxD signal should be:

$$t_{REC} < t_{DBT} + t_{TSEG2}\,(1 + df_B) + t_{CC} - t_{CLK} - t_{safety\ margin}$$

- Supposing that ECU A is slower than ECU B, at the 6th bit of the observed RxD signal should be:

$$t_{REC} > t_{TSEG2}\,(1 - df_B) + t_{CC} + t_{CLK} + t_{safety\ margin}$$

With both inequalities, t_{REC} is bounded between a minimum and a maximum possible value. An automated evaluation should be able to detect if t_{REC} is out of boundaries and report this in the verdict. The reception of own transmitted messages is also an important scenario and need to be considered in an additional validation criterion. Especially in CAN FD communication with the usage of higher bit rates like 2 Mbit/s or 5 Mbit/s, the so-called ‘Transmitter Delay Compensation’ and its secondary sampling point (SSP) is applied at each transmitting node. Due to the fact that a correct sampling of its own transmitted bits is not given anymore, the propagation delays of the transmitting node will be compensated by using this mechanism. This will cause

some specific considerations like an additional quantization error. Additional to that, the internal bit time logic starts during the transmitting process and parts like the wiring propagation delay are omitted. Another important measurement is given by the data settle time criterion. The critical edge here is the state change from dominant to recessive. The measurement could be considered between the higher threshold voltage of 0.9 V and the lower threshold of 0.5 V. The opportunity to include the five dominant bits before changing to the recessive state in the measurement, results in a precise outcome and exact analysis because also the delay of the rising edge is considered. The bus level should be below 500 mV to avoid sampling of the wrong bus state at the latest on the sampling point position.

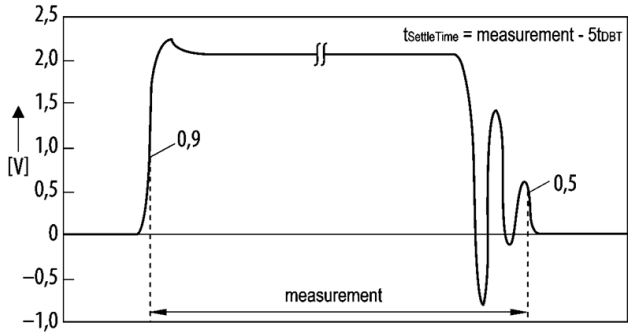

Fig. 4 Data settle time measurement

3. RELIABLE RESULTS VIA VERIFICATION

Each Designer and development department is interested in achieving a certain degree of confidence after simulation results thus the next step in this direction is to execute some laboratory measurements. Important: the ECU and topology design as well as the stimulus and observation points need to be adapted to the simulation. A measurement at a junction connector or at the connector of the ECU cannot be compared to the simulation. Best indicator is given by the curve shape of the differential signal but also the digital signals at the RxD pin of the transceiver could be used. Furthermore, the observation of the error-free communication with real ECUs or test modules could be used to compare the general result (pass or fail condition, which means error frames, problems during the arbitration or bus off state of connected nodes). The verification is considered with the final topology design and conducted before mass production.

4. NEED OF AUTOMATIZATION

It is worth to mention that the maximum bit rate depends on the target topology and therefore each design needs to be validated at a certain bit rate. Supposed that a topology design with 11 nodes is considered, n = 11. At the same time, the topology should be evaluated in 2 Mbit/s and 5 Mbit/s. Due to different temperature conditions within a vehicle as well as the consideration of corner case simulation, the measurement should be done in low, typical and high temperature condition. With a kind of test, described in this paper, basically n^2 signals need to be analyzed to evaluate the behavior on each transmitter/receiver combination. For each signal, two measurements should be taken: one for the analogue signal and one for the recessive bit width. The total required process gives a total of nearly 1500 measurements only for the data phase. The evaluation of the arbitration phase, with some different scenarios, result in additional 1452 measurements. Maybe a single person can do this process alone or working in teams, but how much time and effort is required to generate results for this analysis? Not even mentioned the involved human error. Now another perspective: supposed that one or more connections show many problems.

Now, the network needs to be modified and re-evaluated. With an automated system, all measurements are done in a few hours or even some minutes. With simulation, the problems in the network are well-known and only the important parts need to be measured at the end of the validation process.

5. Conclusion

Recent technology applied to the classical CAN bus allows to perform a communication with a higher data rate and even larger payloads. Simulation nowadays is an excellent approach to overcome the design problems at an early stage of a vehicle development or newer versions of existent designs. The higher data transmission rate makes the asymmetry on different signals within a network a key to success and its evaluation is achievable by means of simulation. On the other side, while simulation alone plays an important role for new CAN FD challenges, automatization is what makes a difference regarding the effectiveness and efficiency of a project. With automatization, not only huge networks can be evaluated but also marginal behaviors due to production tolerance and temperature coefficients are contemplated. With an automatized simulation environment, a topology can be evaluated to different real possible conditions, where various parts of the topology can be exposed to different temperatures; components of each node are affected to fabrication tolerances; cables are affected to different temperatures, which influence the impedance; clock deviation is maximal in some nodes and minimal in others. Simulation through automatization makes it possible for the CAN FD IVN topology designer to manage such effort in a topology validation.

The cost reduction and the broad analysis are two key points that will make the designs better than ever before.